

# JEAN GREY 11.6" Schematic

## Stoney Ridge FT4

2019-03-29

REV : A00

*DY : None Installed*

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<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title

**Cover Page**

Size  
A3

Document Number

**JEAN GREY AMD**

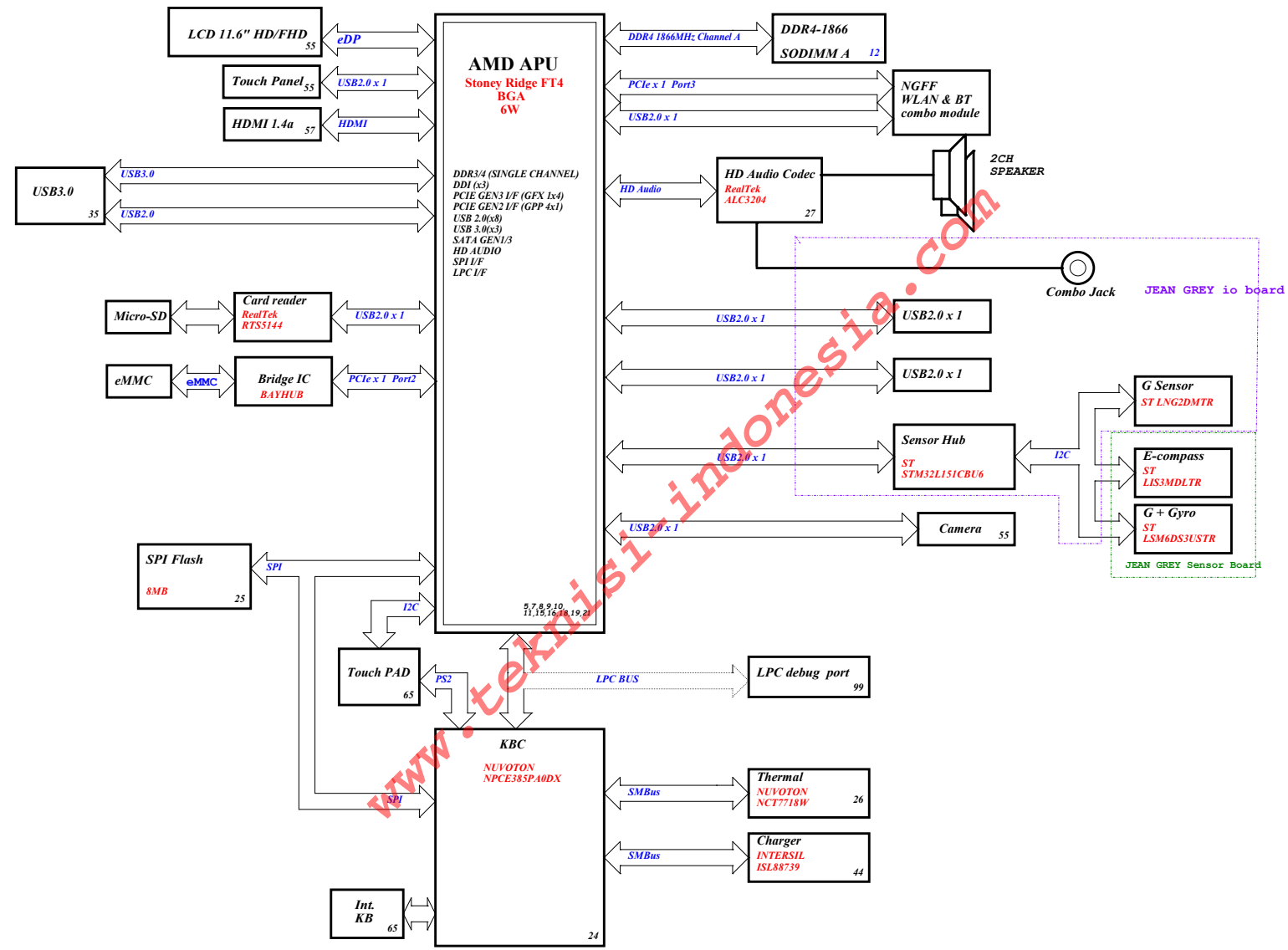
Rev

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# JEAN GREY\_AMD Stoney Ridge Block Diagram

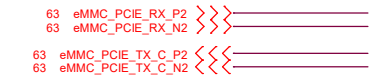


CHARGER		ISL88739HRZ-T	44
INPUTS	OUTPUTS		
AD+ 12V_BT-	DCBATOUT		
SYSTEM DC/DC		RT6575D6QW	45
INPUTS	OUTPUTS		
DCBATOUT	3D3V_AUX_S5	3D3V_S5	5V_AUX_S5
CPU Core Power		ISL62771HRTZ	46-47
INPUTS	OUTPUTS		
DCBATOUT	1V_CPU_CORE	1D2V_CPU_VDDNB	
DDR4 SUS		G5388K11U	53
INPUTS	OUTPUTS		
DCBATOUT	1D2V_S3		
CPU VDDP		G5388K11U	52
INPUTS	OUTPUTS		
DCBATOUT	0D95V_S5		
CPU VDD18		RT5797AL6QW	54
INPUTS	OUTPUTS		
3D3V_S5	1D8V_S5	3D3V_AUX_S5	1D8V_AUX_S5
CPU VDDCR6FX		APL5337KAI	49
INPUTS	OUTPUTS		
1D8V_S5	0D775V_S5		
Switches			40
INPUTS	OUTPUTS		
5V_S5	5V_S0	3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0	0D95V_S5	0D95V_S0

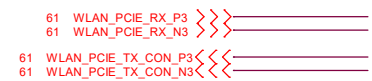
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

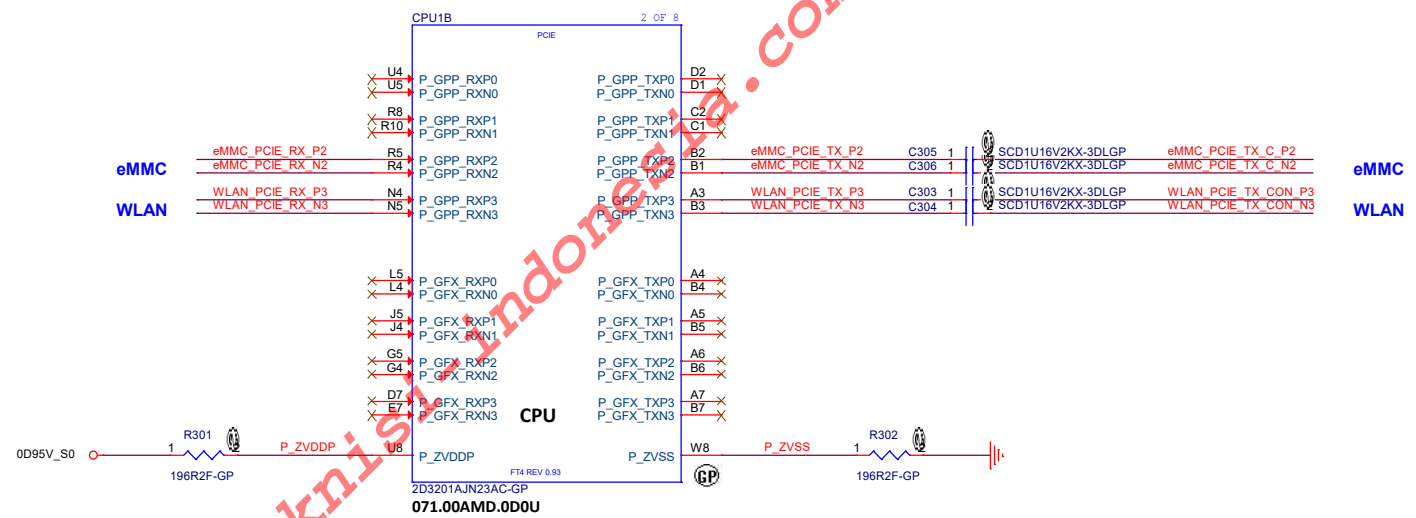
eMMC



WLAN



GPP CLK port	Device	CLKREQ#
2	eMMC	2
3	WLAN	3



SSID = CPU

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Title (Reserved)			
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Title			
CPU_(DDR)			
Size A2	Document Number	Rev	
	JEAN GREY AMD	A0	
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SSID = CPU

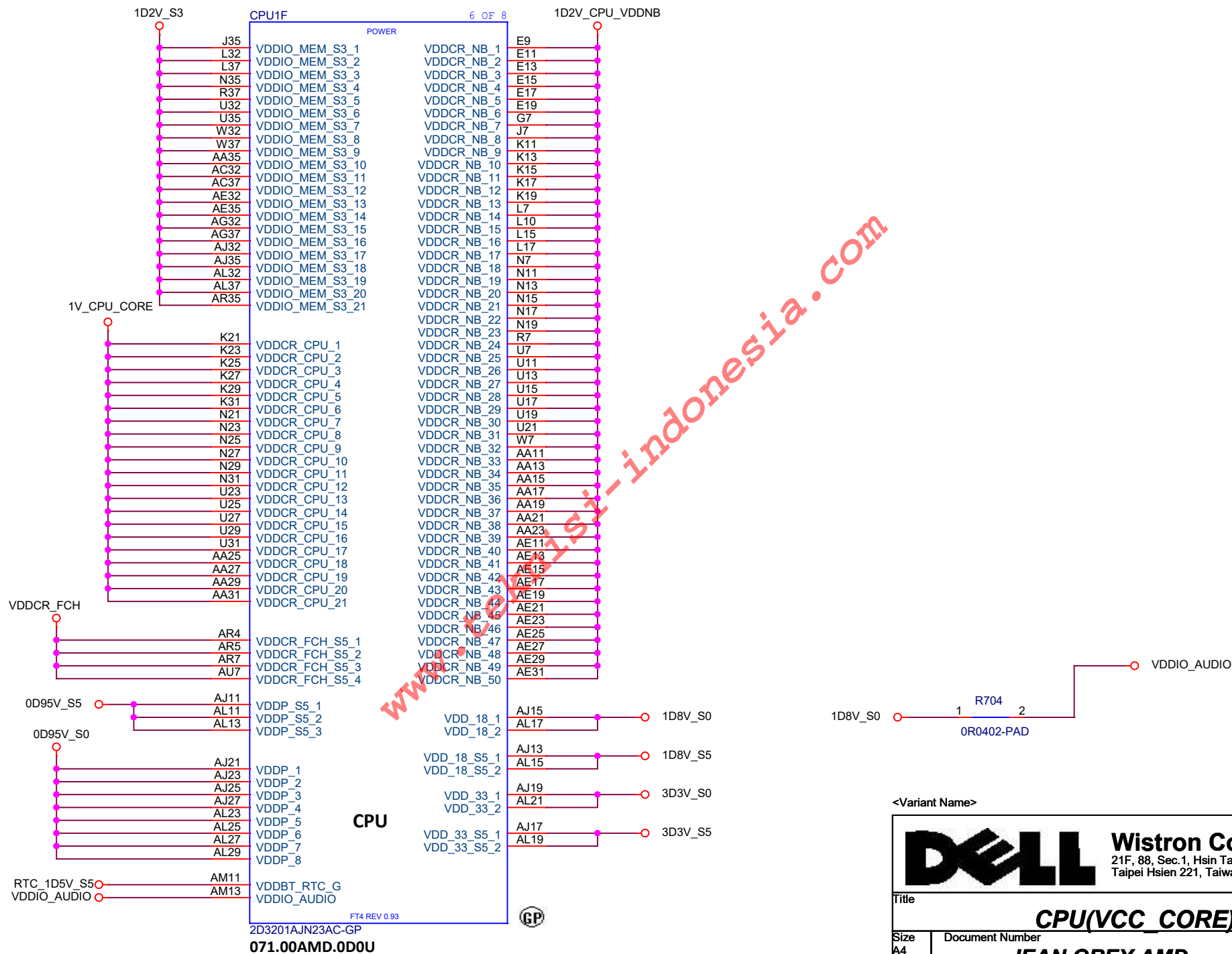
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SSID = CPU



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Title

**CPU(VCC\_CORE)**

Size  
A4

Document Number

**JEAN GREY AMD**

Rev  
**A00**

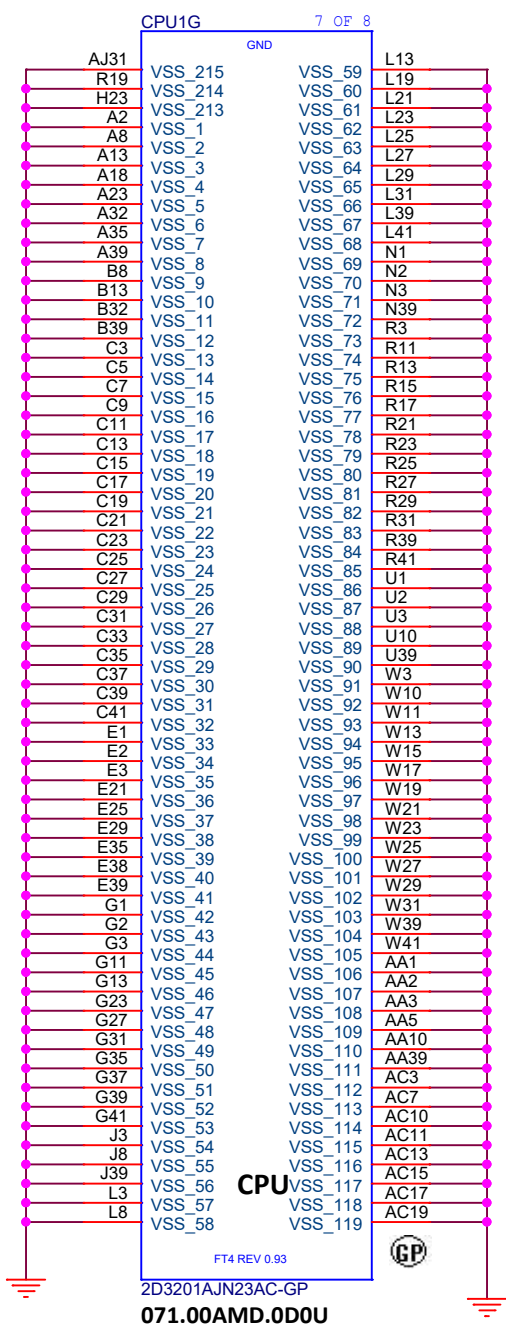
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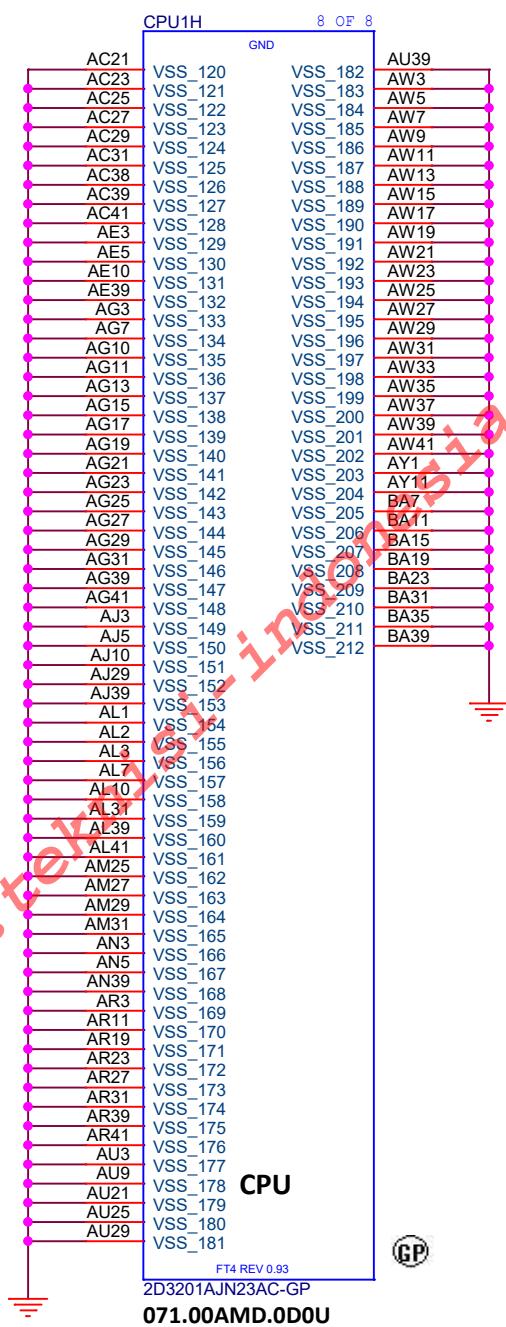
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Title <b>CPU (DISPLAY/SV12 JTAG/TEST)</b>	
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SSID = CPU



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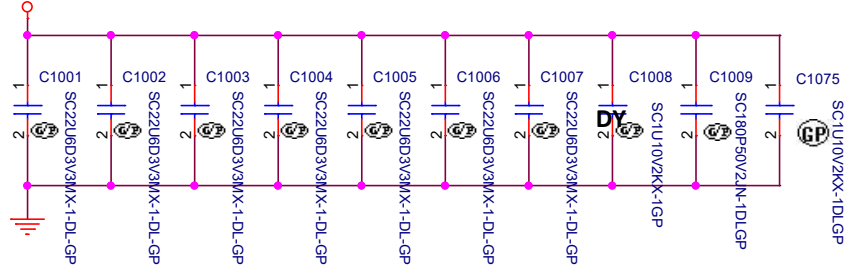
Title **CPU (VSS)**

Size A4	Document Number <b>JEAN GREY AMD</b>	Rev <b>A00</b>
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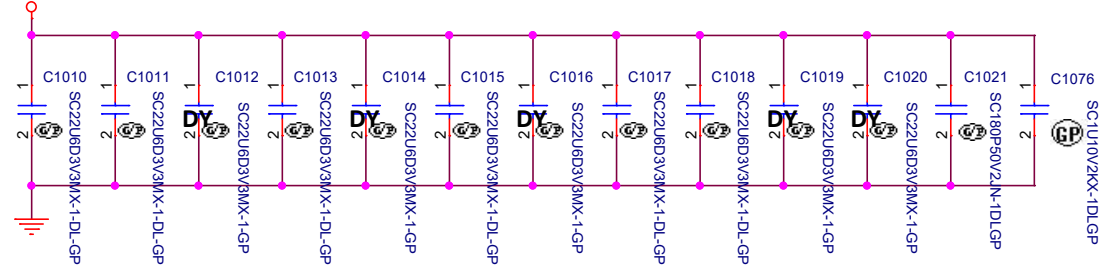
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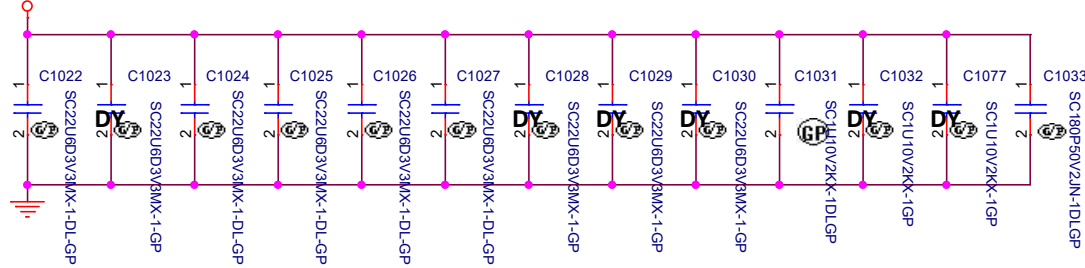
1V\_CPU\_CORE



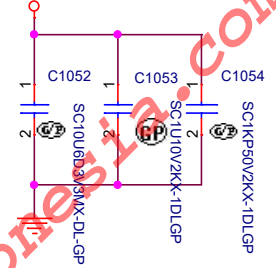
1D2V\_CPU\_VDDNB



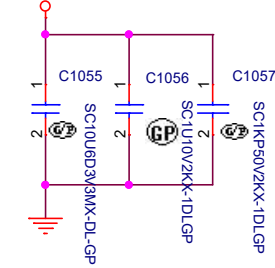
1D2V\_S3



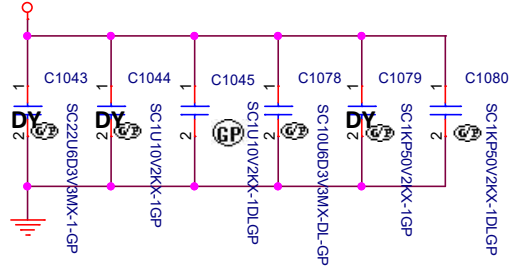
1D8V\_S5



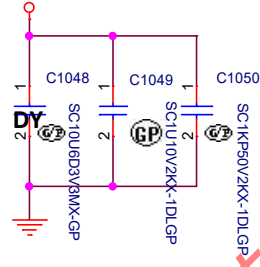
1D8V\_S0



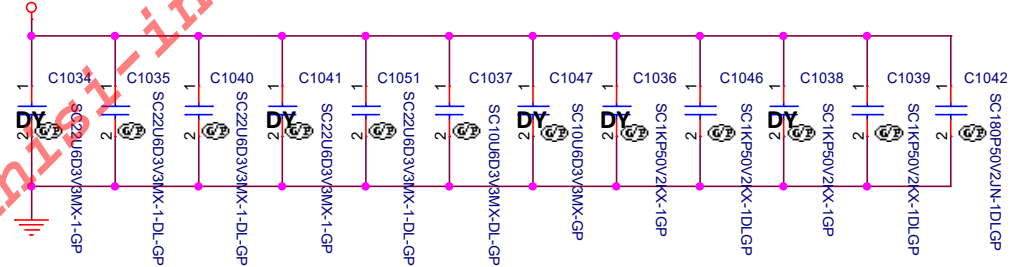
VDDCR\_FCH



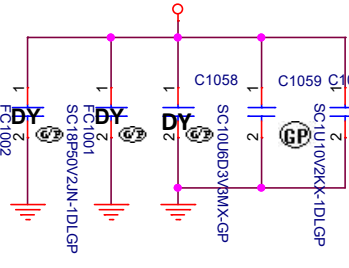
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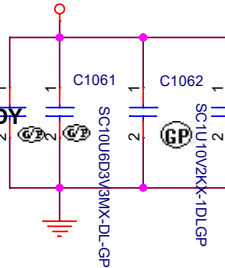
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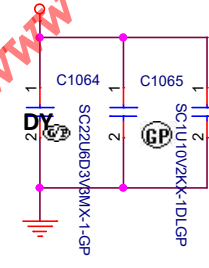
3D3V\_S5



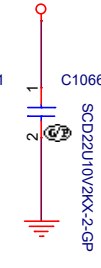
3D3V\_S0



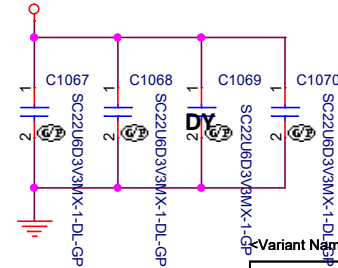
VDDIO\_AUDIO



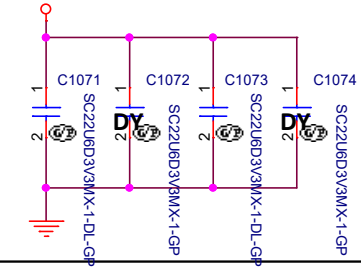
RTC\_1D5V\_S5



1V\_CPU\_CORE



1D2V\_CPU\_VDDNB



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CPU (Power CAP1)			
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SSID = CPU

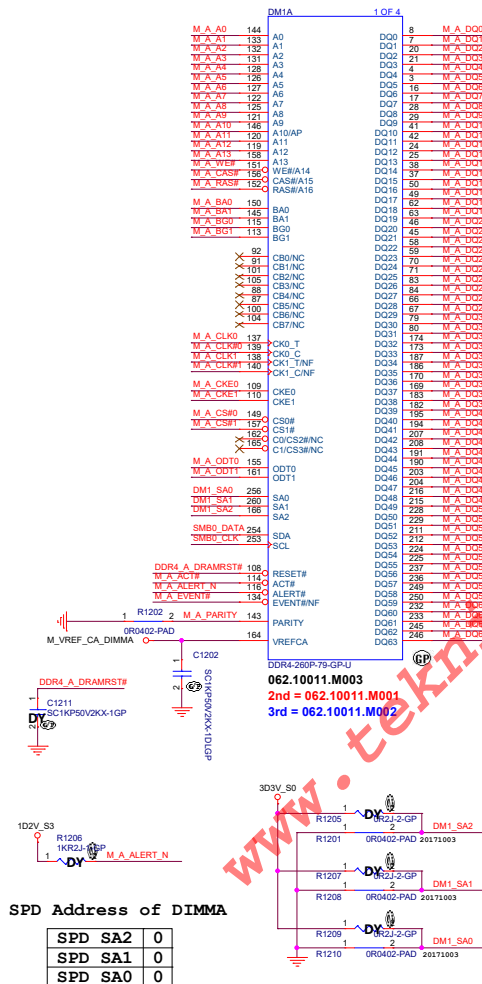
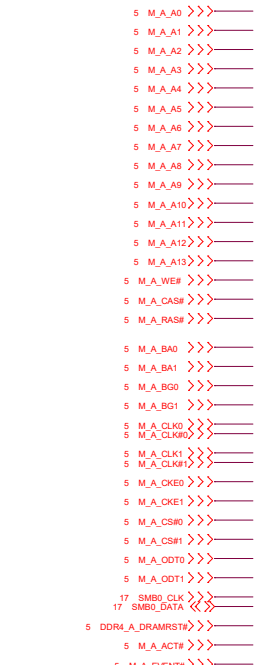
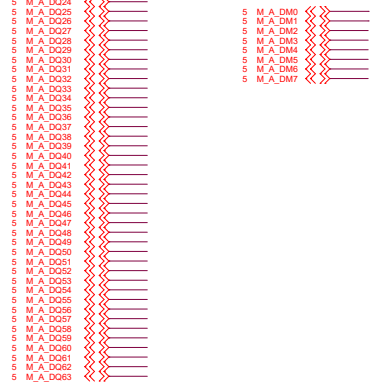
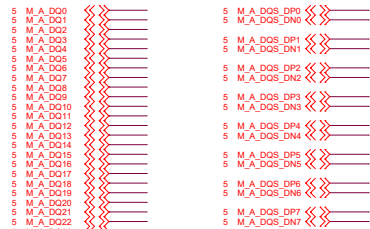
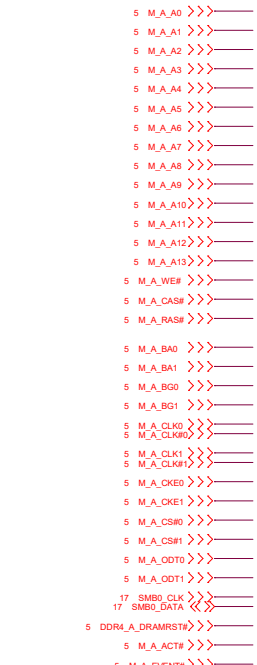
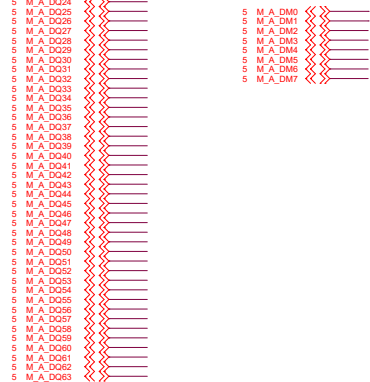
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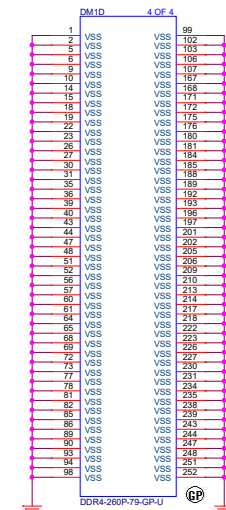
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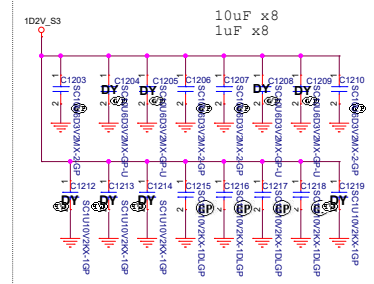
5	M_A_D00		5	M_A_D05_DP0	
5	M_A_D01		5	M_A_D05_DP1	
5	M_A_D02		5	M_A_D05_DP11	
5	M_A_D03		5	M_A_D05_DP2	
5	M_A_D04		5	M_A_D05_DP21	
5	M_A_D05		5	M_A_D05_DP3	
5	M_A_D06		5	M_A_D05_DP31	
5	M_A_D07		5	M_A_D05_DP4	
5	M_A_D08		5	M_A_D05_DP41	
5	M_A_D09		5	M_A_D05_DP5	
5	M_A_D10		5	M_A_D05_DP51	
5	M_A_D11		5	M_A_D05_DP6	
5	M_A_D12		5	M_A_D05_DP61	
5	M_A_D13		5	M_A_D05_DP7	
5	M_A_D14		5	M_A_D05_DP71	
5	M_A_D15		5	M_A_D05_DP8	
5	M_A_D16		5	M_A_D05_DP81	
5	M_A_D17		5	M_A_D05_DP9	
5	M_A_D18		5	M_A_D05_DP91	
5	M_A_D19		5	M_A_D05_DP10	
5	M_A_D20		5	M_A_D05_DP101	
5	M_A_D21		5	M_A_D05_DP11	
5	M_A_D22		5	M_A_D05_DP111	



SPD	SA2	0
SPD	SA1	0
SPD	SA0	0



Layout Note :  
Place these Caps near DIM1




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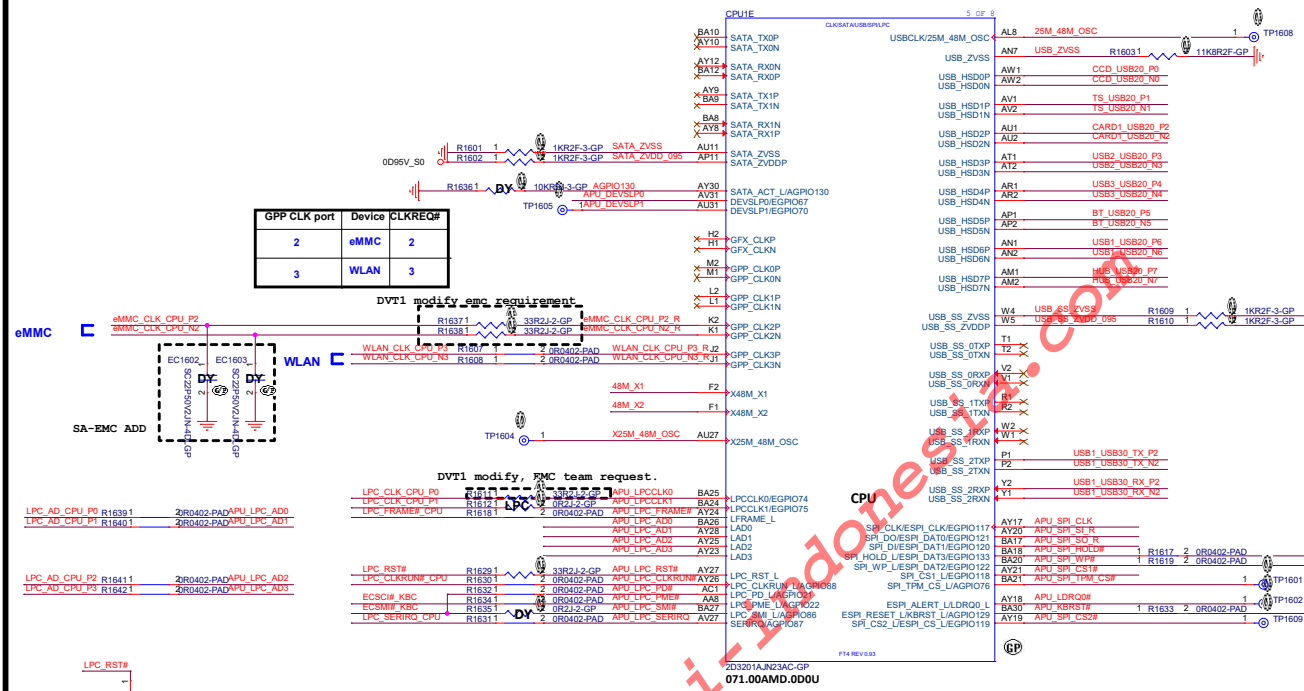
55 CCD\_USB20\_P0 <<<>>>  
55 CCD\_USB20\_N0 <<<>>>  
55 TS\_USB20\_P1 <<<>>>  
55 TS\_USB20\_N1 <<<>>>  
33 CARD1\_USB20\_P2 <<<>>>  
33 CARD1\_USB20\_N2 <<<>>>  
66 USB2\_USB20\_P3 <<<>>>  
66 USB2\_USB20\_N3 <<<>>>  
66 USB3\_USB20\_P4 <<<>>>  
66 USB3\_USB20\_N4 <<<>>>  
61 BT\_USB20\_P5 <<<>>>  
61 BT\_USB20\_N6 <<<>>>  
35 USB1\_USB20\_P6 <<<>>>  
35 USB1\_USB20\_N6 <<<>>>  
66 HUB\_USB20\_P7 <<<>>>  
66 HUB\_USB20\_N7 <<<>>>  
35 USB1\_USB30\_TX\_P2 <<<>>>  
35 USB1\_USB30\_TX\_N2 <<<>>>  
35 USB1\_USB30\_RX\_P2 <<<>>>  
35 USB1\_USB30\_RX\_N2 <<<>>>

63 eMMC\_CLK\_CPU\_P2 <<<>>>  
63 eMMC\_CLK\_CPU\_N2 <<<>>>  
61 WLAN\_CLK\_CPU\_P3 <<<>>>  
61 WLAN\_CLK\_CPU\_N3 <<<>>>

20 APU\_LPCCLK1 <<<>>>  
24 KBRST# <<<>>>

20,24 LPC\_CLK\_CPU\_P0 <<<>>>  
68 LPC\_CLK\_CPU\_P1 <<<>>>  
20,24,68 LPC\_FRAME#\_CPU <<<>>>  
24,68 LPC\_RST# <<<>>>  
24 LPC\_CLKRUN#\_CPU <<<>>>  
24 ECSCM#\_KBC <<<>>>  
24 ECSCM#\_KBC <<<>>>  
24 LPC\_SERIRQ\_CPU <<<>>>  
24,68 LPC\_AD\_CPU\_P0 <<<>>>  
24,68 LPC\_AD\_CPU\_P1 <<<>>>  
24,68 LPC\_AD\_CPU\_P2 <<<>>>  
24,68 LPC\_AD\_CPU\_P3 <<<>>>

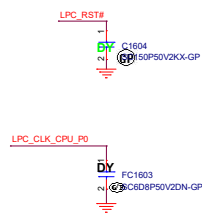
25 SPI\_HOLD\_CPU <<<>>>  
25 SPI\_WP\_CPU <<<>>>  
24,25 SPI\_CLK\_ROM <<<>>>  
24,25 SPI\_SI\_ROM <<<>>>  
24,25 SPI\_SO\_CPU <<<>>>  
24,25 SPI\_CS\_ROM\_N0 <<<>>>



GPP CLK port	Device	CLKREQ#
2	eMMC	2
3	WLAN	3

DVT1 modify emc requirement

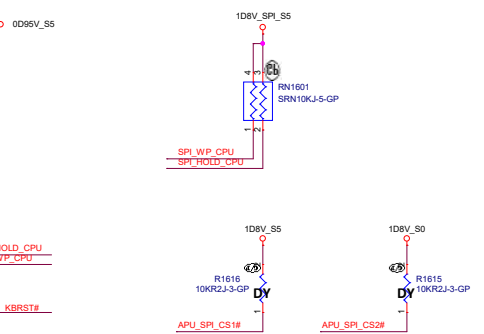
DVT1 modify emc team request



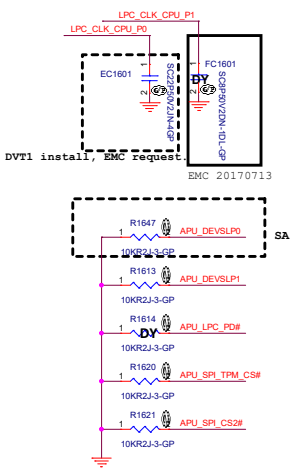
	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M

### USB Table

Pair	Device
0	camera
1	Touch Panel (IOBD Conn.)
2	Card Reader
3	USB2.0 (IOBD Conn.)
4	USB2.0 (IOBD Conn.)
5	BT (NGFF)
6	USB3.0 (MB port2)
7	Sensor Hub (IOBD Conn.)
0	NA
1	NA
2	USB3.0 (MB port2)



APU\_SPI\_CLK R16431 2/R0402-PAD SPI\_CLK\_ROM  
APU\_SPI\_SI\_R R16441 2/R0402-PAD SPI\_SI\_ROM  
APU\_SPI\_SO\_R R16451 2/R0402-PAD SPI\_SO\_CPU  
APU\_SPI\_CS1# R16461 2/R0402-PAD SPI\_CS\_ROM\_N0



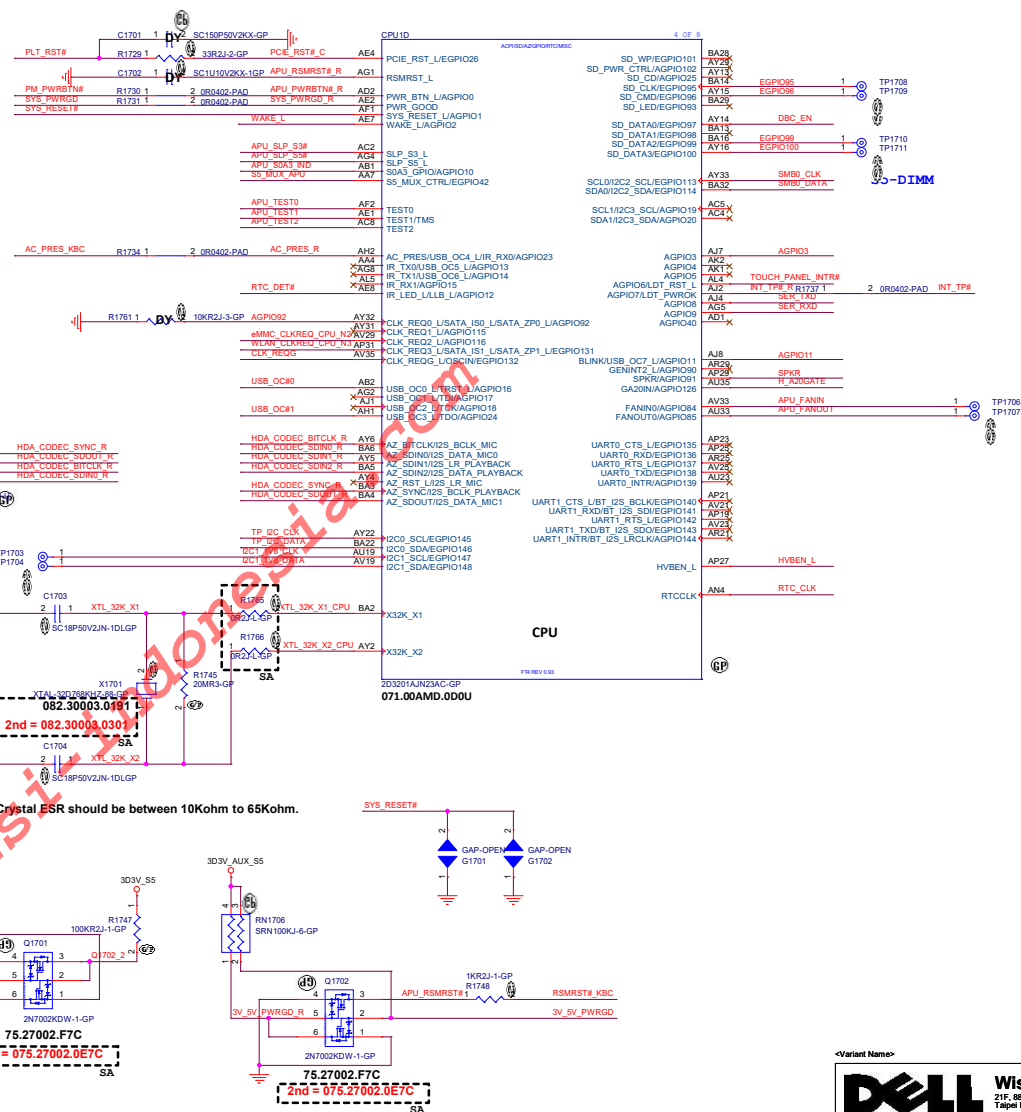
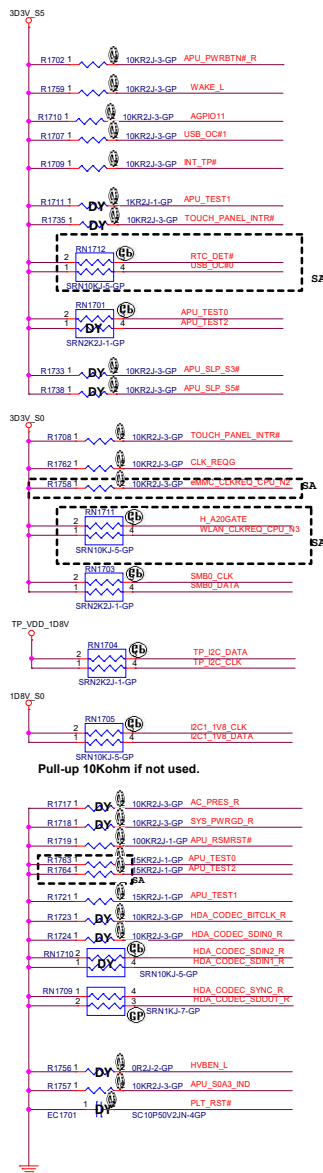
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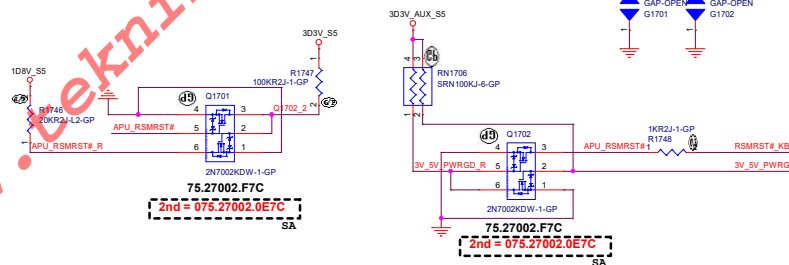
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01.63.68  PLT_RST# <<<
20  SYS_RESET# <<<
24  PMU_PWRBTN# >>>
24.26.40  SYS_PWRGD <<<
24.40.53  APU_SLP_S# >>>
24.44.53  APU_SLP_S# >>>
40  S5_MUX_APU <<<
24  AC_PRES_KBC <<<
25  RTC_DET# <<<
44  eMMC_CKREQ_CPU_0,N2 >>>
WLAN_CKREQ_CPU_0,N3 >>>
66  USB_OC# <<<
36  USB_OC#1 <<<
27  HDA_SYNC_CODECD <<<
27  HDA_SDOUT_CODECD <<<
27  HDA_BITCLK_CODECD <<<
27  HDA_SDO#_CPU >>>
65  TP_OC_CLK <<<
65  TP_OC_DATA <<<
24  RSMRST#_KBC >>>
45.49.54  3V_SW_PWRGD <<<
55  DRC_EN <<<
12  SMB0_CLK <<<
12  SMB0_DATA <<<
20  AGPIO3 >>>
TOUCH_PANEL_INT# >>>
65  INT_TP# >>>
61  SER_TXD <<<
61  SER_RXD <<<
27  SPI# <<<
24  H_AGGATE <<<
20  RTC_CLK <<<

```



**Crystal ESR should be between 10Kohm to 65Kohm.**



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Title

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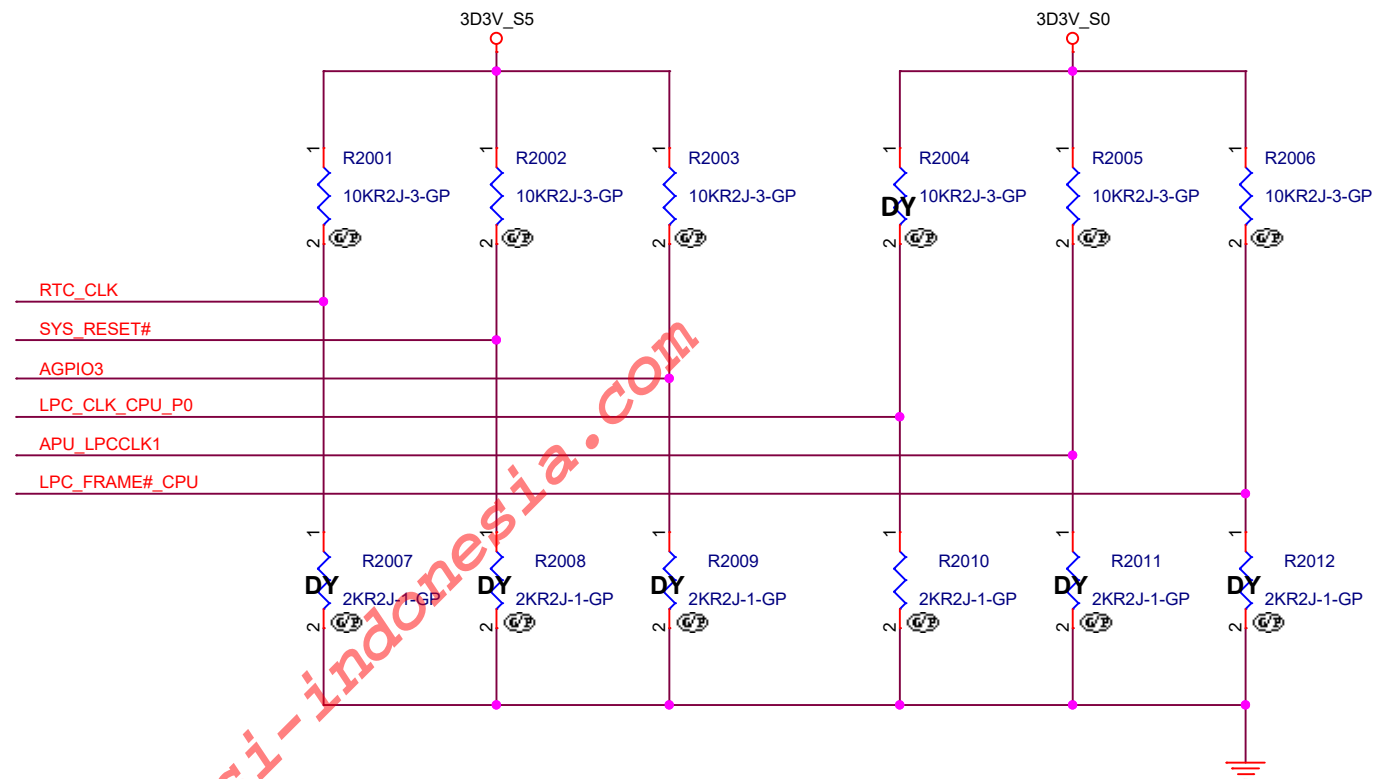
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# SSID = STRAPING

17 RTC\_CLK <<<—  
17 SYS\_RESET# <<<—  
17 AGPIO3 <<<—  
16,24 LPC\_CLK\_CPU\_P0 <<<—  
16 APU\_LPCCLK1 <<<—  
16,24,68 LPC\_FRAME#\_CPU <<<—

## SYSTEM STRAPPINGS



## REQUIRED SYSTEM STRAPS

	RTC_CLK	SYS_RESET#	AGPIO3	LPC_CLK0	LPC_CLK1	LPC_FRAME#
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

<Variant Name>



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Title

**CPU Strappings**

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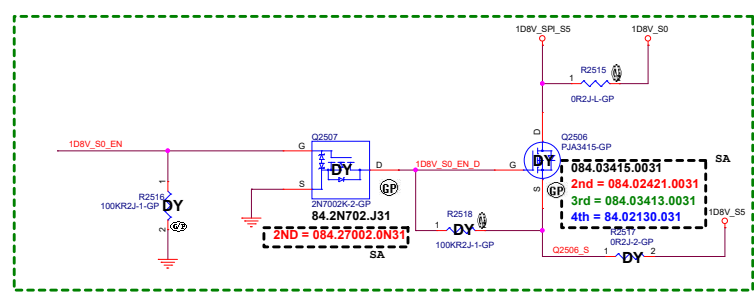
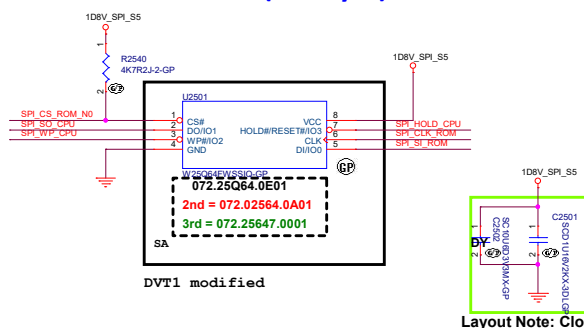
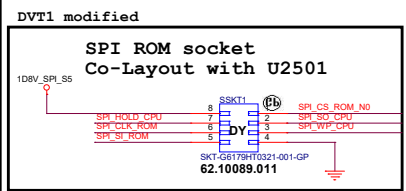




SSID = Flash.ROM

16 SPI\_HOLD\_CPU >>> \_\_\_\_\_  
16.24 SPI\_CLK\_ROM >>> \_\_\_\_\_  
16.24 SPI\_SI\_ROM >>> \_\_\_\_\_  
16.24 SPI\_CS\_ROM\_N0 >>> \_\_\_\_\_  
16.24 SPI\_SO\_CPU <<< \_\_\_\_\_  
16 SPI\_WP\_CPU <<< \_\_\_\_\_  
40 1D8V\_S0\_EN >>> \_\_\_\_\_

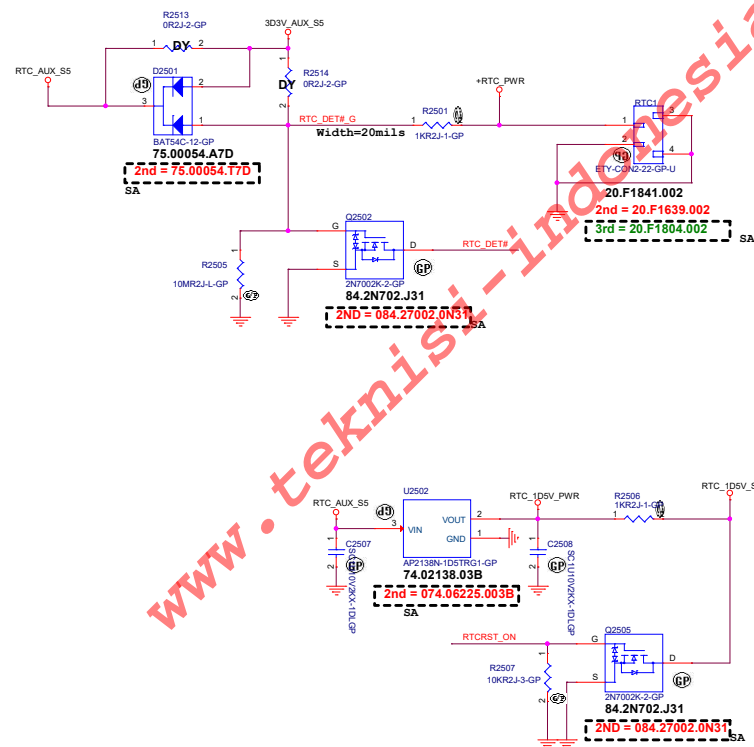
SPI FLASH ROM (8M byte) for CPU



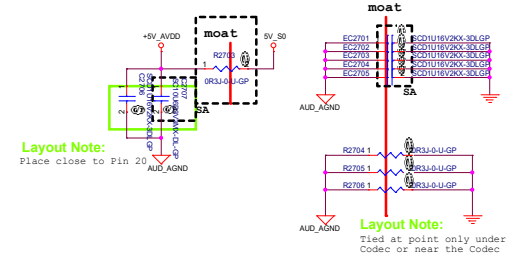
Layout Note: Close to U2501 Pin 8


SSID = RTC

17 RTC\_DET# <<< \_\_\_\_\_  
24 RTCRST\_ON >>> \_\_\_\_\_








**Layout Note:**   
Tied at point only under  
Codec or near the Codec

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<Variant Name>

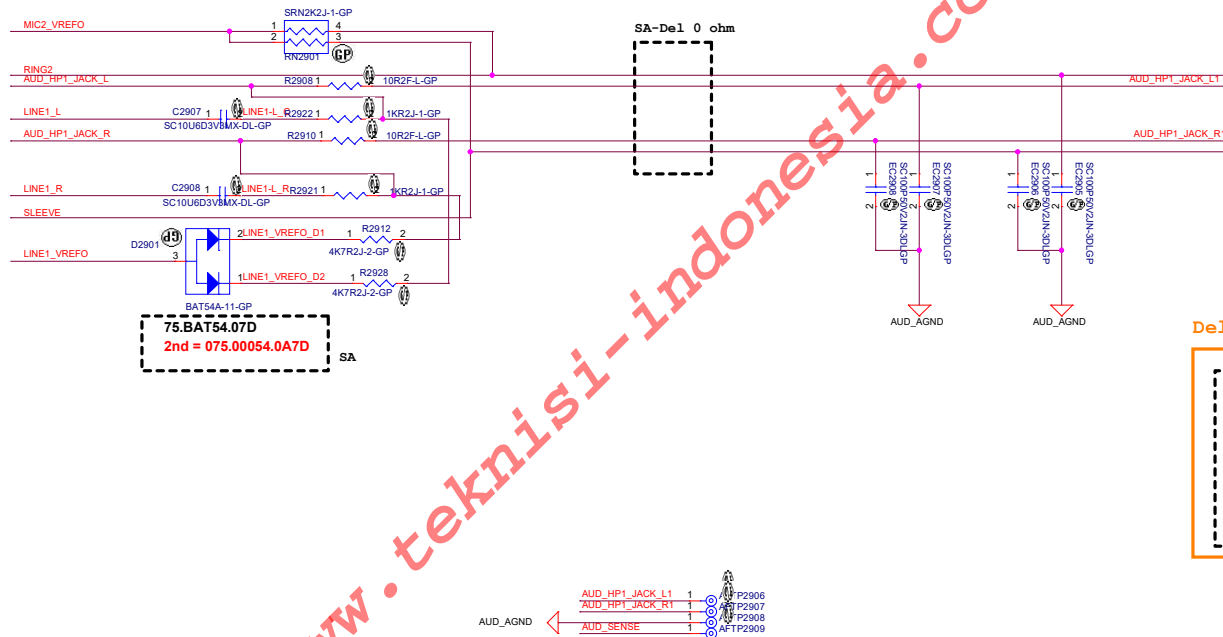
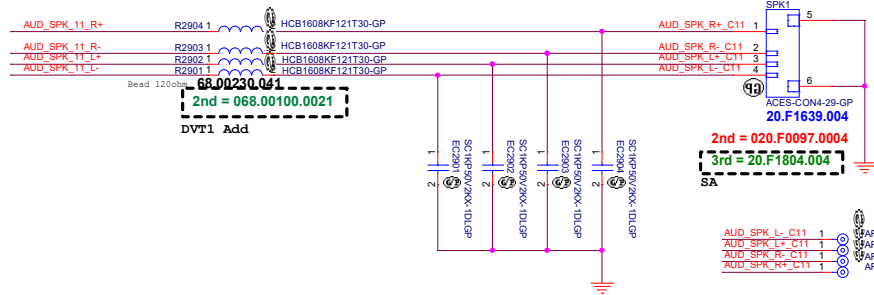
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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SSID = AUDIO

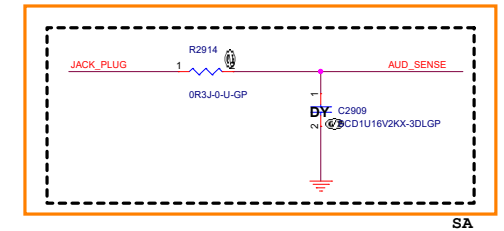
27 AUD\_SPK\_11\_R+ >>>  
27 AUD\_SPK\_11\_R- >>>  
27 AUD\_SPK\_11\_L+ >>>  
27 AUD\_SPK\_11\_L- >>>

27 MIC\_VREF0 >>>  
27 RING2 <<<  
27 AUD\_HP1\_JACK\_L >>>  
27 LINE1\_L <<<  
27 AUD\_HP1\_JACK\_R >>>  
27 LINE1\_R <<<  
27 SLEEVE <<<  
27 LINE1\_VREF0 >>>  
27 AUD\_SENSE <<<

66 JACK\_PLUG >>>  
66 RING2 >>>  
66 AUD\_HP1\_JACK\_L1 <<<  
66 AUD\_HP1\_JACK\_R1 <<<  
66 SLEEVE >>>



Delay circuit



<Variant Name>

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Title  
**Speaker/HPMIC CONN**  
Size Custom Document Number  
**JEAN GREY AMD** Rev  
**A00**  
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<Variant Name>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved)LOM**

Size  
A4

Document Number

**JEAN GREY AMD**

Rev  
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<Variant Name>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **(Reserved)LAN**


Size A4	Document Number <b>JEAN GREY AMD</b>	Rev <b>A00</b>
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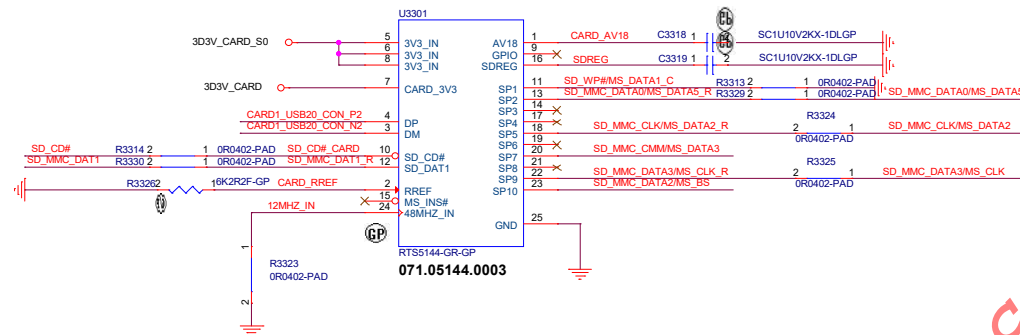
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<Variant Name>

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Title <b>(Reserved)RJ45+Transformer</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
Date: Tuesday, April 02, 2019		Sheet 32 of	109

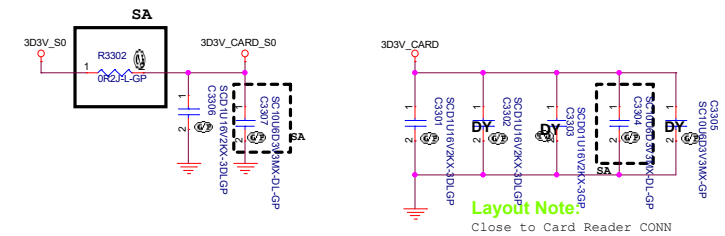
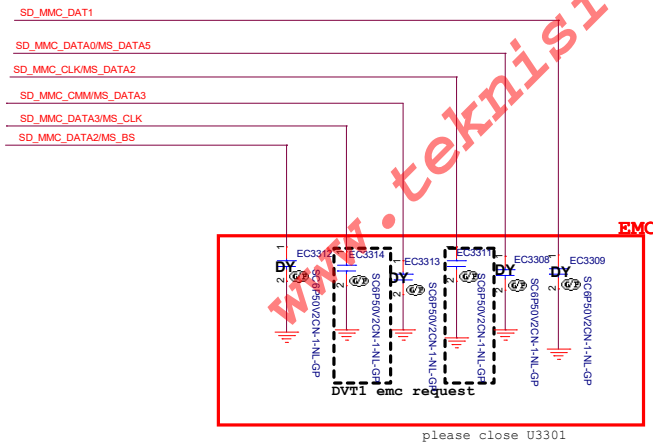


16 CARD1\_USB20\_P2 <<>>  
16 CARD1\_USB20\_N2 <<>>



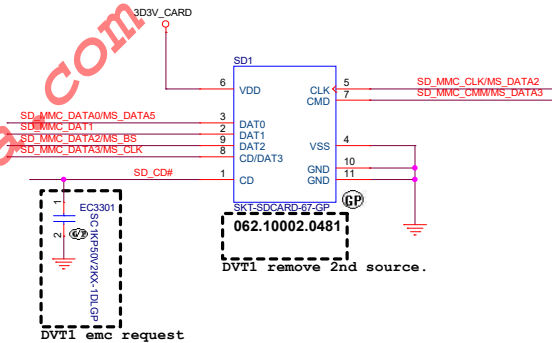
Net name	
Pin name	
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS

For EMI Reserved

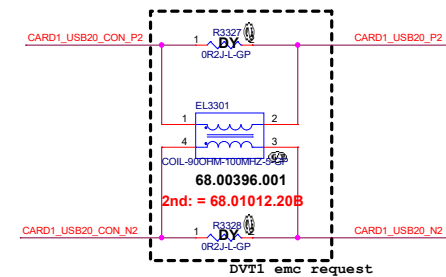


**Layout Note:**

Close to Card Reader CONN



Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



**<Variant Name>**



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Title	<b>Card Reader + CONN</b>
-------	---------------------------


Size	Document Number	Rev
Custom	<b>JEAN GREY AMD</b>	<b>A00</b>

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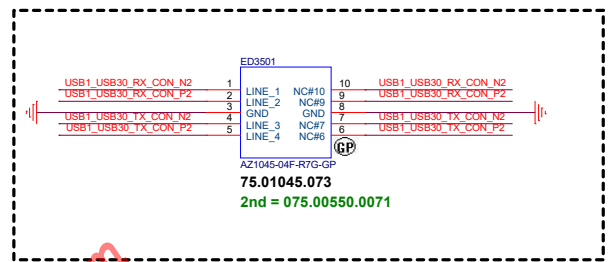
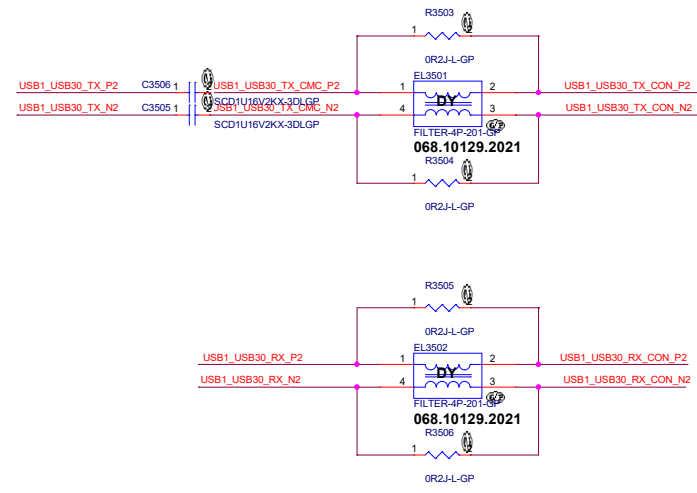
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<Variant Name>

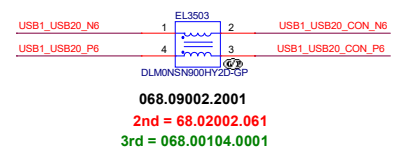
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)USB 2.0 Port</b>		
Size A4	Document Number <b>JEAN GREY AMD</b>	Rev <b>A00</b>
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SSID = USB

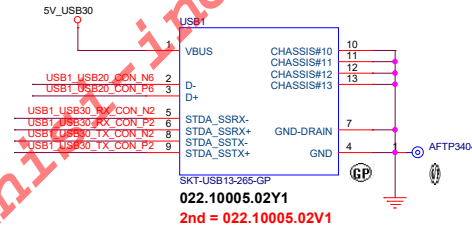
16 USB1\_USB30\_TX\_P2 >>>>  
16 USB1\_USB30\_TX\_N2 >>>>  
16 USB1\_USB30\_RX\_P2 <<<<  
16 USB1\_USB30\_RX\_N2 <<<<  
16 USB1\_USB20\_P6 <<<<  
16 USB1\_USB20\_N6 <<<<



DVT1

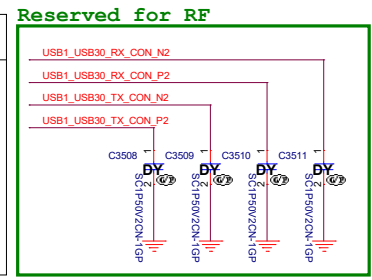


068.09002.2001  
2nd = 68.02002.061  
3rd = 068.00104.0001

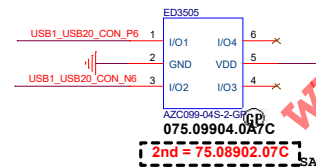


022.10005.02Y1  
2nd = 022.10005.02V1

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



Reserved for RF



075.09904.0A7C  
2nd = 75.08902.07C

<Variant Name>

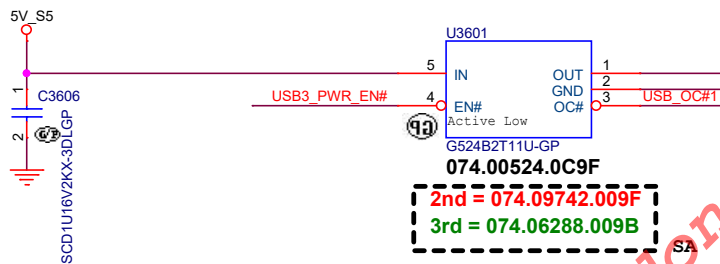
**Wistron Corporation**  
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Title <b>USB3.0 CONN</b>		
Size	Document Number <b>JEAN GREY AMD</b>	Rev <b>A00</b>
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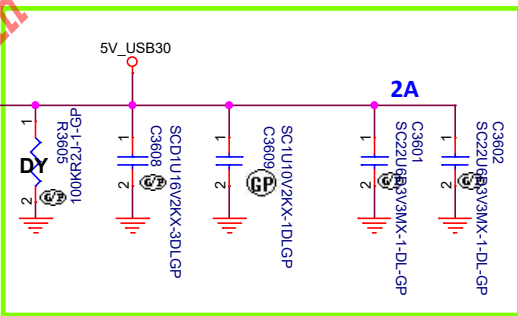
SSID = USB

24 USB3\_PWR\_EN# >>>—  
17 USB\_OC#1 <<<—


USB3.0 Port1



Layout Note: Close CON1




<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>USB Power SW</b>			
Size Custom	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB2.0 HUB</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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<Variant Name>



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Title

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<Variant Name>



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Title

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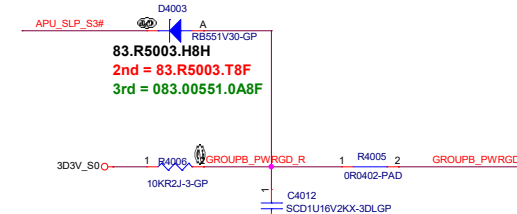
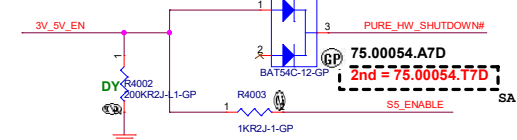
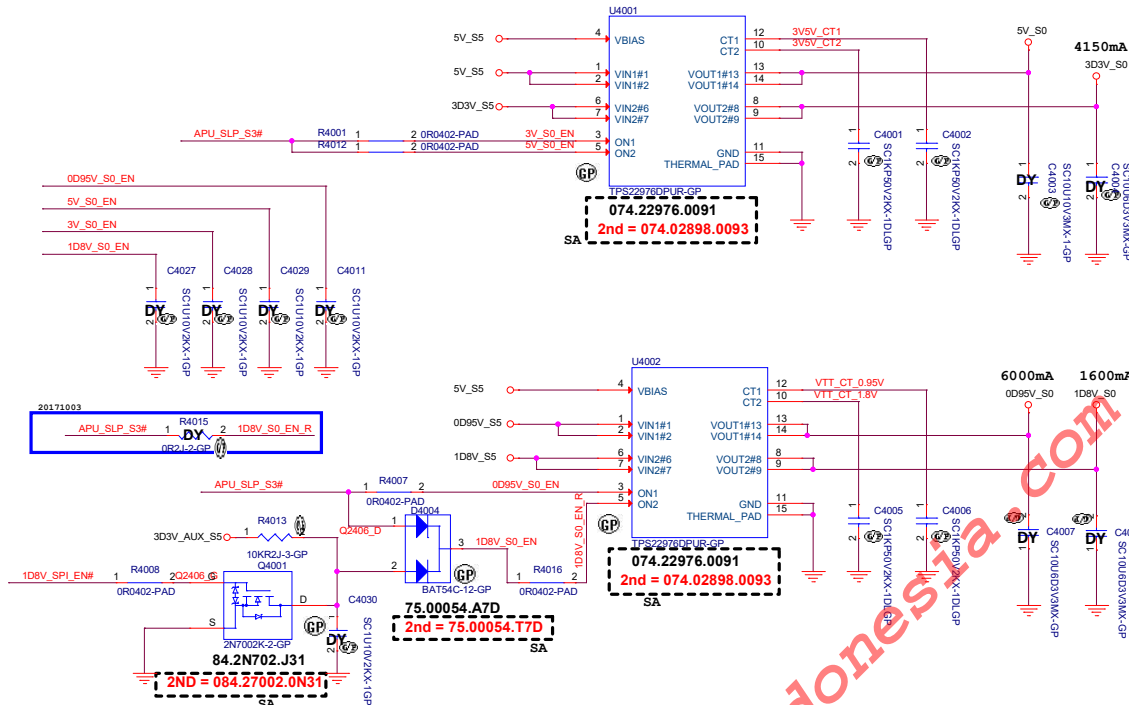
Rev  
**A00**

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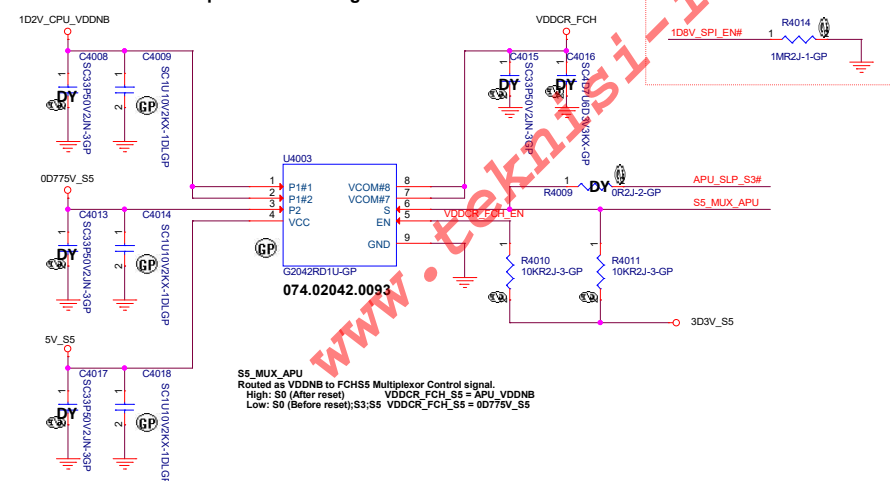
# Power Sequence

17,24,53 APU\_SLP\_S3# >>>  
 25 1D8V\_S0\_EN >>>  
 24 1D8V\_S0\_EN# >>>  
 17 S5\_MUX\_APU <<<  
 45 3V\_S0\_EN <<<  
 24,26 PURE\_HW\_SHUTDOWN# >>>  
 24 S5\_ENABLE >>>  
 17,24,26 SYS\_PWRGD <<<  
 46 GROUPB\_PWRGD <<<



Delay for S0\_PWRGD to VCORE\_EN

## VDDNB to FCHS5 Multiplexor Control signal



DVT2: Add 1M ohm Pull-down on 1D8V\_S0\_EN# 7/18

VCC	EN	S	P1 Voltage	Function
5	0	X	X	Both P1 and P2 do not pass to VCOM. VCOM is with pull low R of 200 Ω
5	1	0	< P2	P2 passed to VCOM
5	1	0	> P2	P1 passed to VCOM
5	1	1	< 2.0V	P1 passed to VCOM

"X" means don't care

Table 148. S5\_MUX\_CTRL State Table

Platform Power State	S5_MUX_CTRL Signal Level	SLP_S3_L	SLP_S5_L	VDDCR_FCH_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON (= VDDCR_FCH_ALW)
S3	0	0	1	ON (= VDDCR_FCH_ALW)
S0, but still in Reset	0	1	1	ON (= VDDCR_FCH_ALW) or if VDDCR_NB ≥ VDDCR_FCH_ALW, tracks VDDCR_NB
S0	1	1	1	Tracks VDDCR_NB

<Variant Name>

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## Power Plane Enable&Sequence

Size: Custom  
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<Variant Name>



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A4

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Title

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Size  
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Document Number

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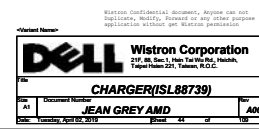
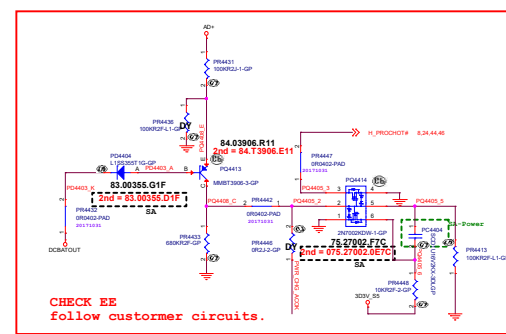
Rev  
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Date: Tuesday, April 02, 2019

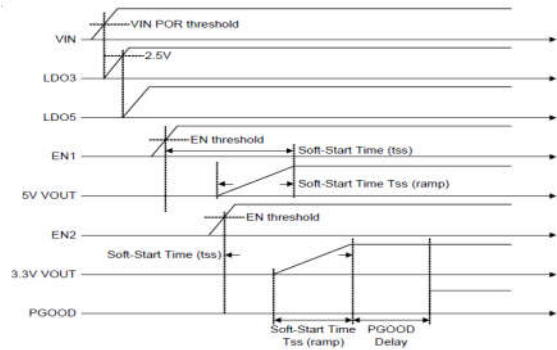
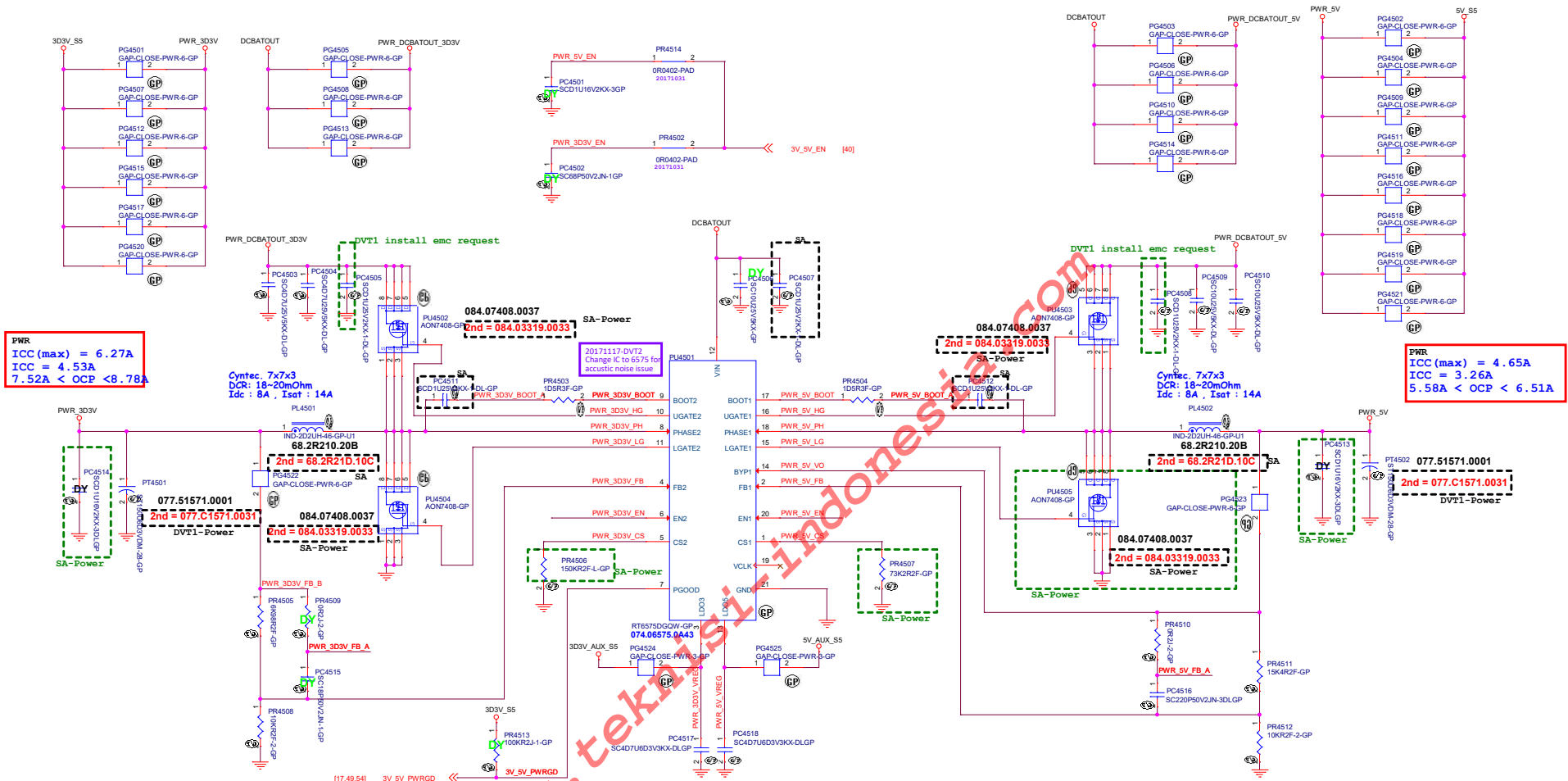
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The diagram illustrates the power supply architecture for a 1U rack-mountable server. It features a 12V 10A power supply (PWR1) and a 12V 10A battery (BAT1) connected to a 12V 10A fuse (F1) and a 12V 10A relay (R1). The schematic shows the internal wiring and component placement for a 12V system. Key components include a 12V 10A power supply (PWR1), a 12V 10A battery (BAT1), a 12V 10A fuse (F1), and a 12V 10A relay (R1). The schematic also shows the connection of various components like capacitors, diodes, and resistors. A large red watermark 'www.teknisi-indonesia.com' is overlaid diagonally across the diagram.



SSID = PWR.Plane.Regulator\_5v3p3v

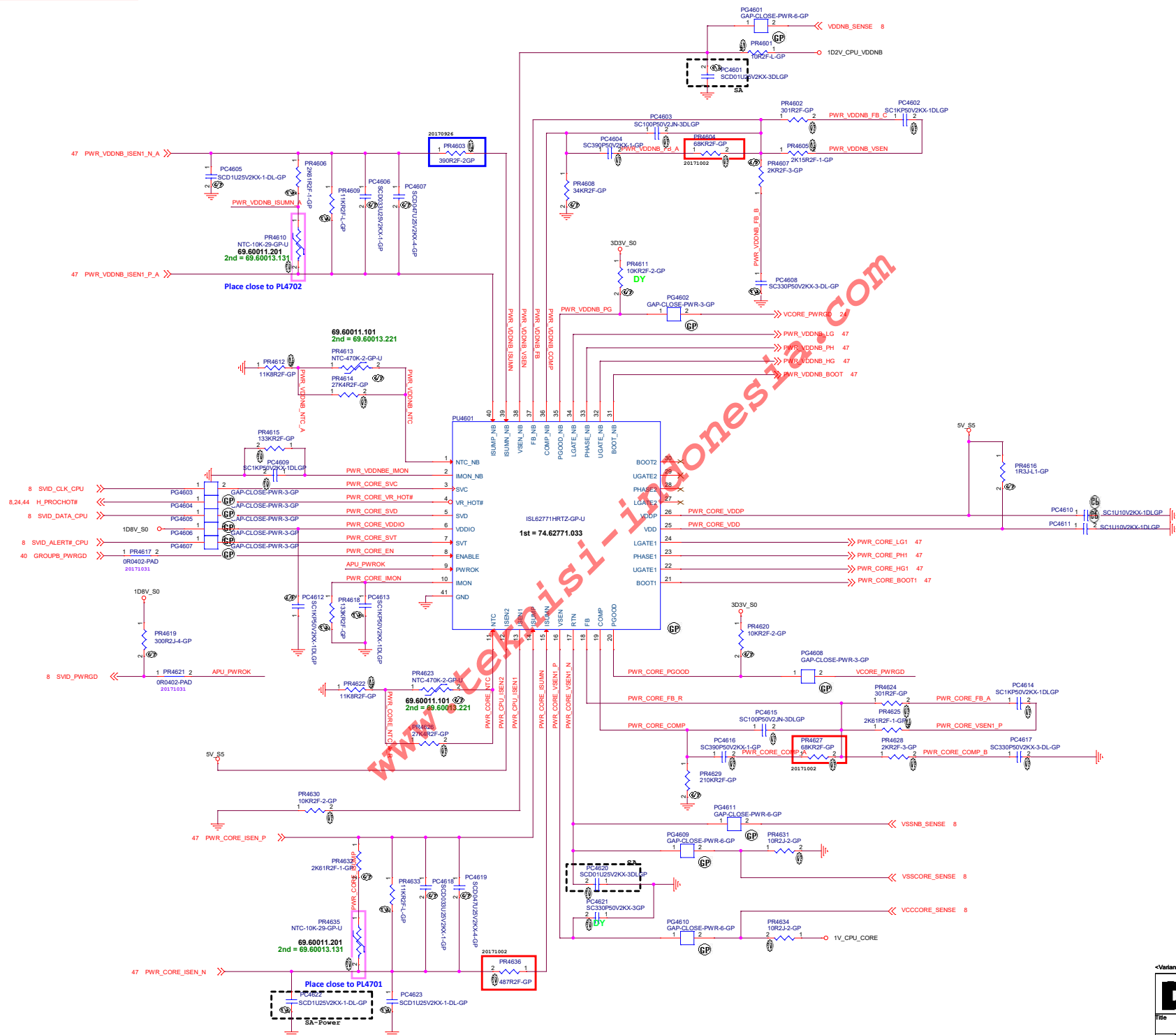


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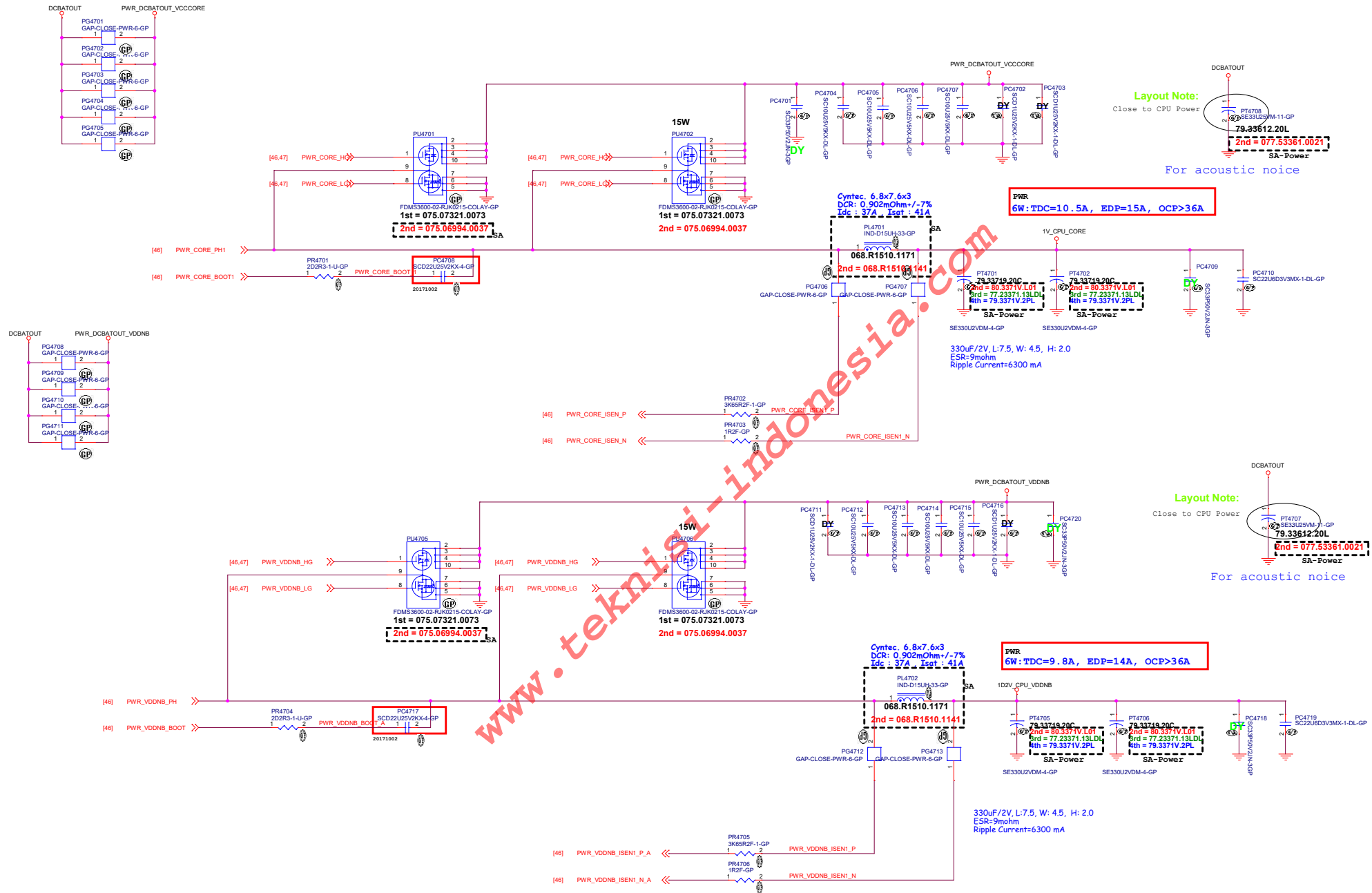
**DELL** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsein 221, Taiwan, R.O.C.

Part Number  
**RT6575 5V/3D3V**  
 JEAN GREY AMD  
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```
SSID = CPU.Regulator
```



SSID = CPU.Regulator




<Variant Name>

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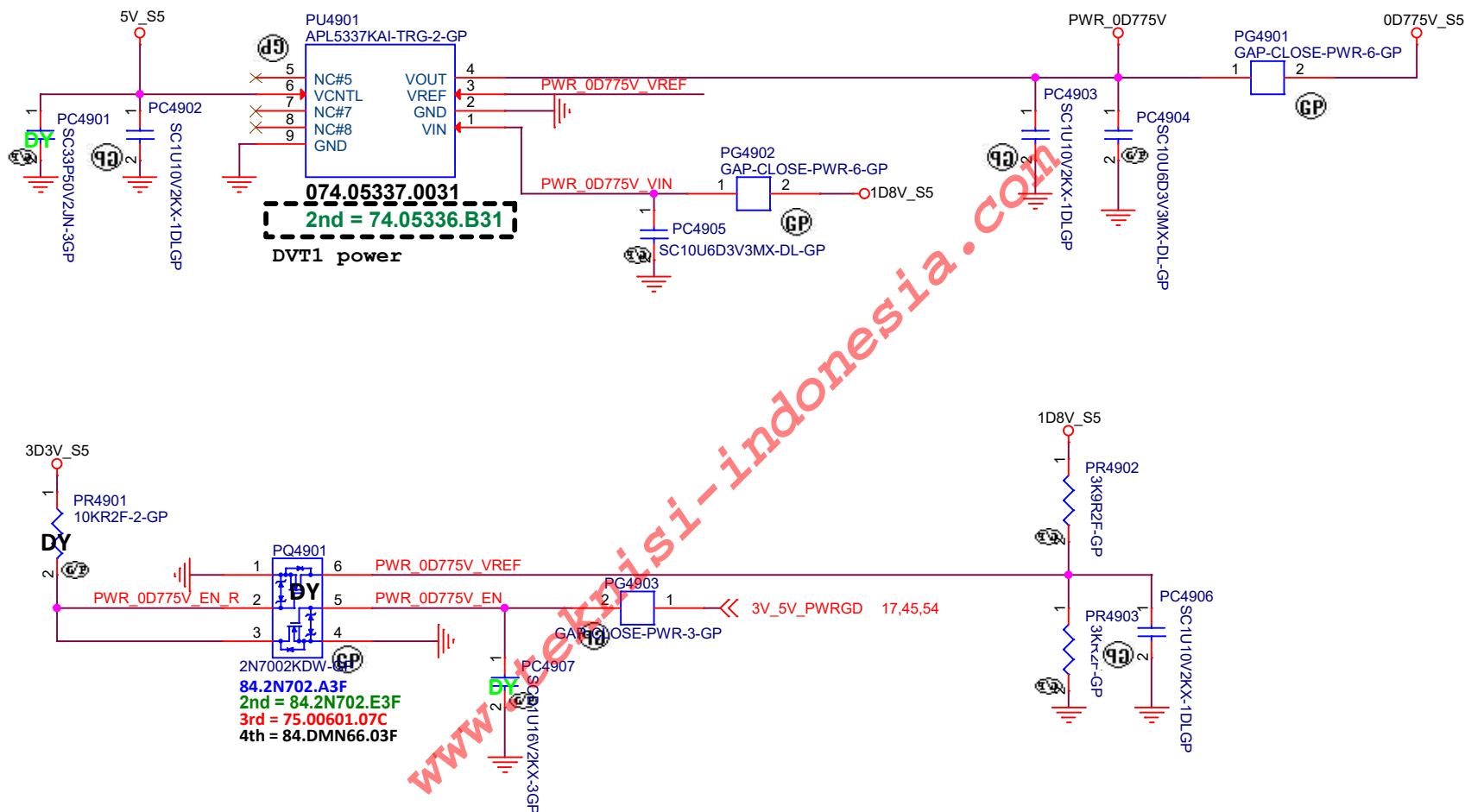
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Title <b>(Reserved)</b>					
Size A4	Document Number <b>JEAN GREY AMD</b>				Rev <b>A00</b>
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SSID = CPU (0D775V)

PWR  
ICC = 70mA  
ICC(max) = 100mA  
VDDCR\_FCH\_S5=0.775V



<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

VDDCRGFX\_APL5337

Size  
A4

Document Number

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<Variant Name>

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Title <b>(Reserved)</b>		
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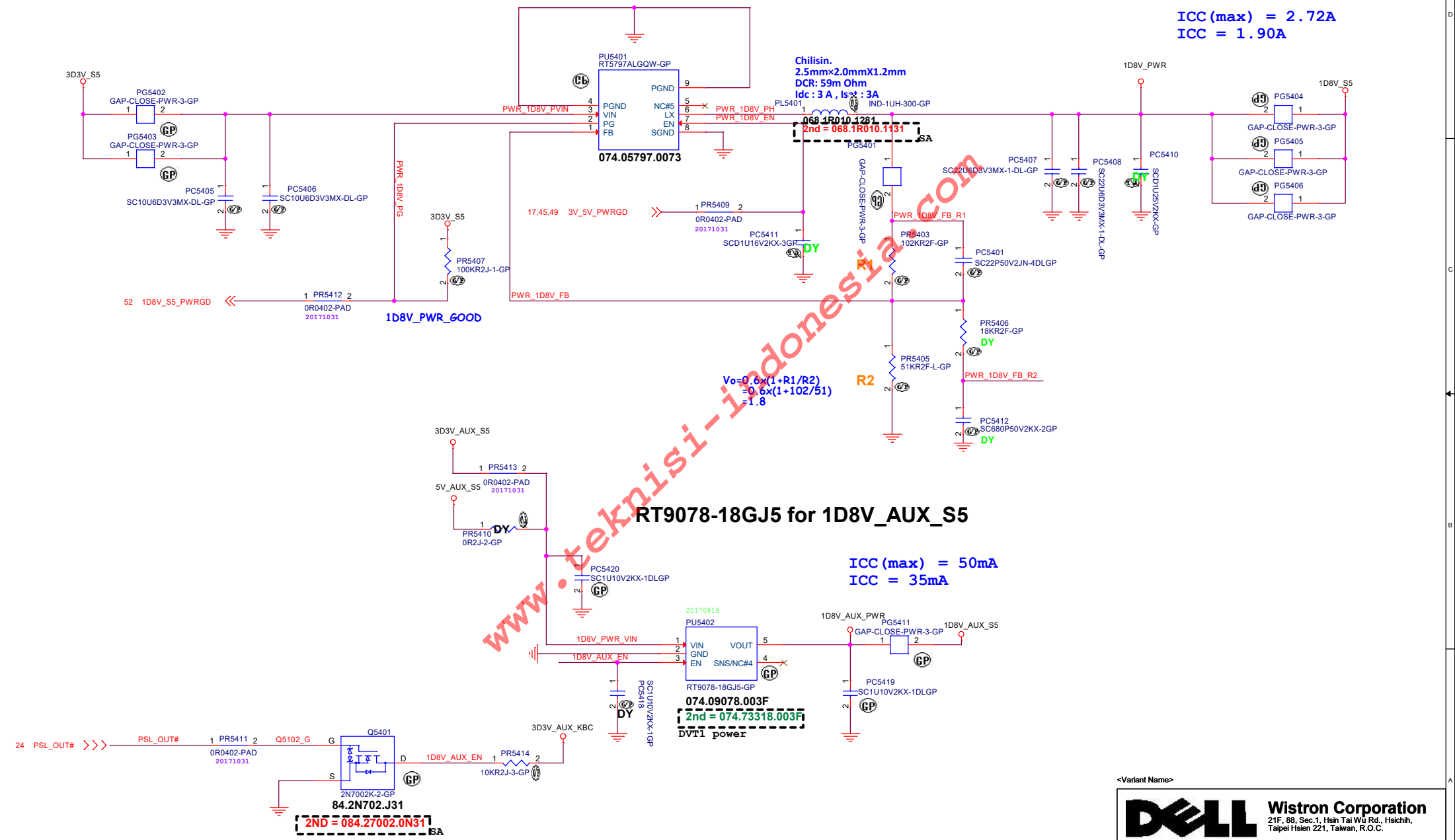
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Title <b>(Reserved)</b>					
Size A4		Document Number <b>JEAN GREY AMD</b>			Rev <b>A00</b>
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SSID = PWR.Plane.Regulator\_1p5v\_1p8v






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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>(Reserved)</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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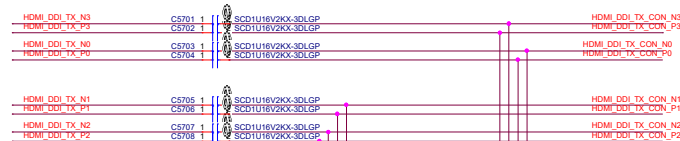


SSID = HDMI

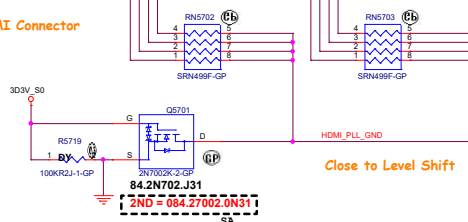
8	HDMI_DDI_TX_P0	↔
8	HDMI_DDI_TX_N0	↔
8	HDMI_DDI_TX_P1	↔
8	HDMI_DDI_TX_N1	↔
8	HDMI_DDI_TX_P2	↔
8	HDMI_DDI_TX_N2	↔
8	HDMI_DDI_TX_P3	↔
8	HDMI_DDI_TX_N3	↔
8	HDMI_SCL_CPU	↔
8	HDMI_SDA_CPU	↔
24	HDMI_IN#	<<<
8	HDMI_DET_CPU	<<<

## HDMI Level Shifter & CONNECTOR

Follow Standard Net Naming rule



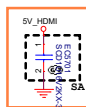
Close to HDMI Connector



### Close to Level Shift

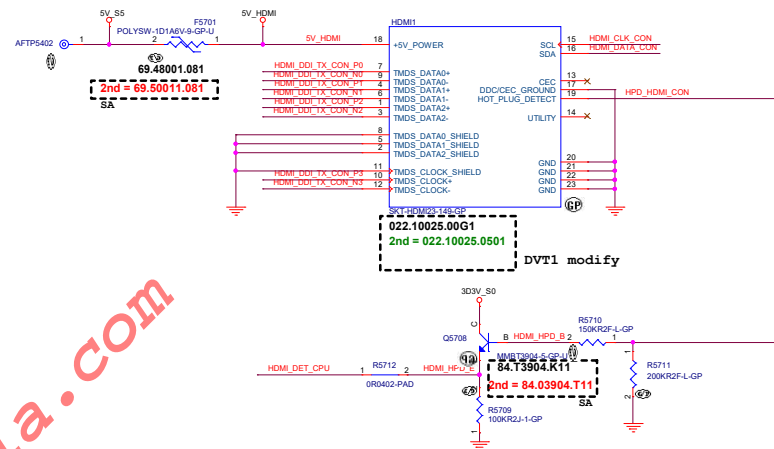


Reserve 150 ohm bridge resistance  
on the HDMI trace as circle for EMI

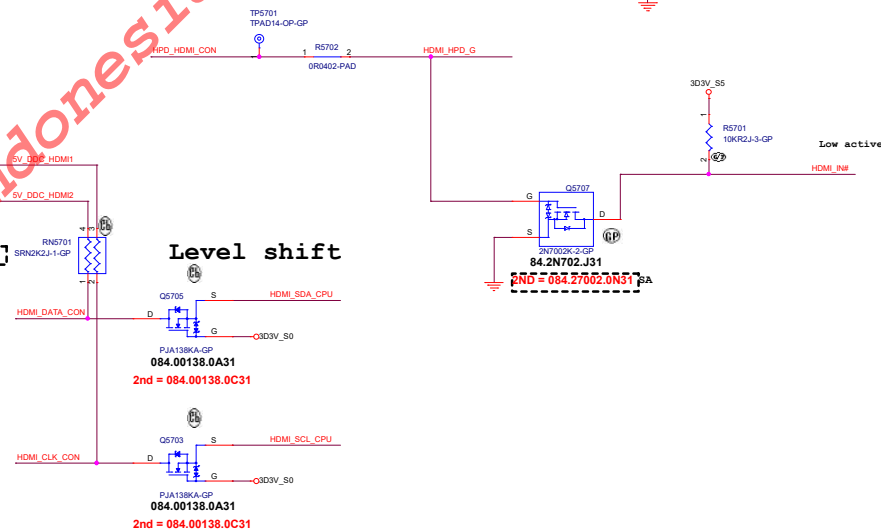


Reserve 0.1uF for ESD

## HDMI CONN



1 modify



## Level shift

<Variant Name>


**DELL** **Wistron Corporation**  
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Title			
<b>HDMI Level Shifter/Connector</b>			
Size	Document Number	Rev	
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved) Display Port</b>			
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# Blanking


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<Variant Name>

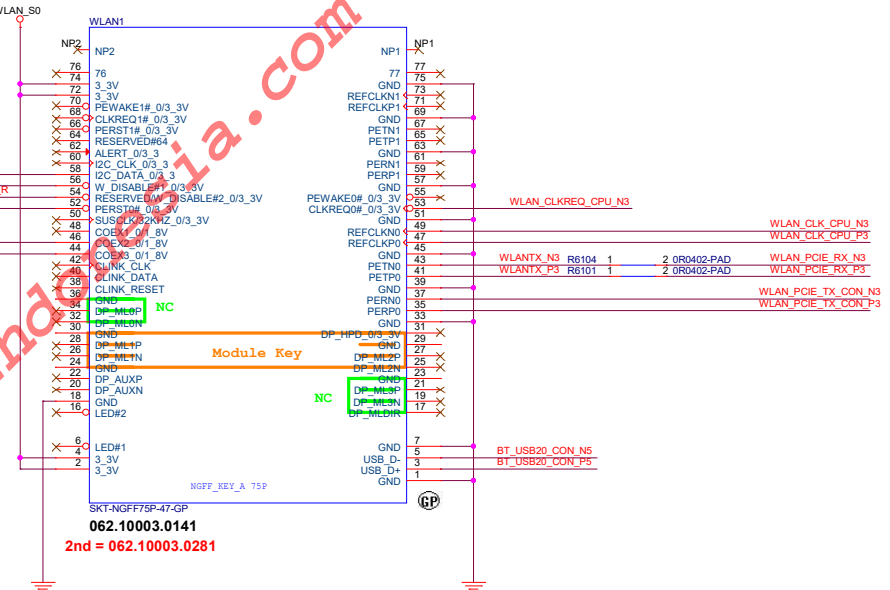
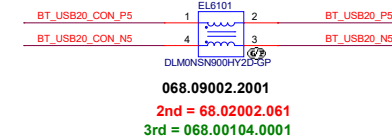
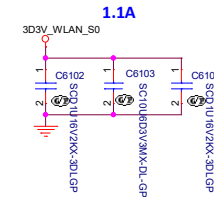
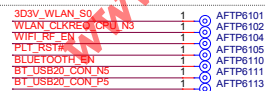
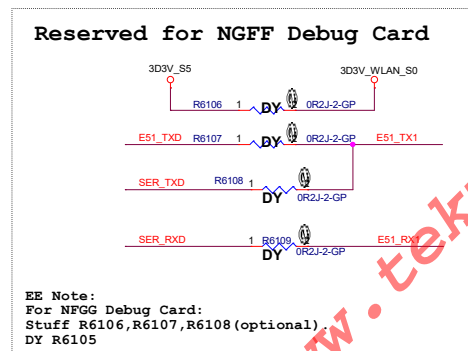
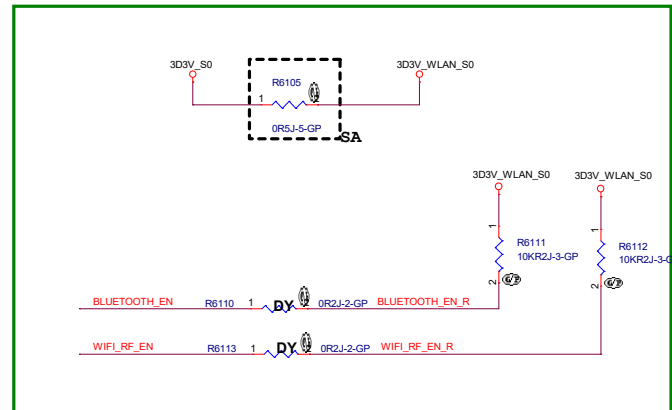
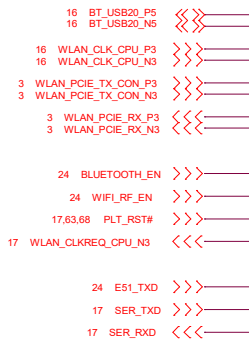
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Title <b>(Reserved) DVI</b>			
Size	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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<Variant Name>		
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Title <b>HDD</b>		
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SSID = WLAN



**<Variant Name>**



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **WLAN**


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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved) WWAN</b>			
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```

16 eMMC_CLK_CPU_P2 >>>
16 eMMC_CLK_CPU_N2 >>>

3 eMMC_PCIE_TX_C_P2 >>>
3 eMMC_PCIE_TX_C_N2 >>>

3 eMMC_PCIE_RX_P2 <<<
3 eMMC_PCIE_RX_N2 <<<

7 eMMC_CLKREQ_CPU_N2 >>>

17.61.68 PLT_RST# >>>


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<Variant Name>

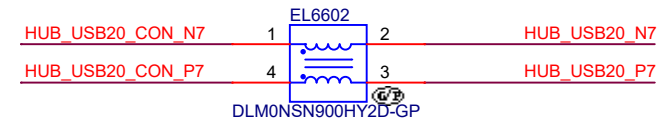
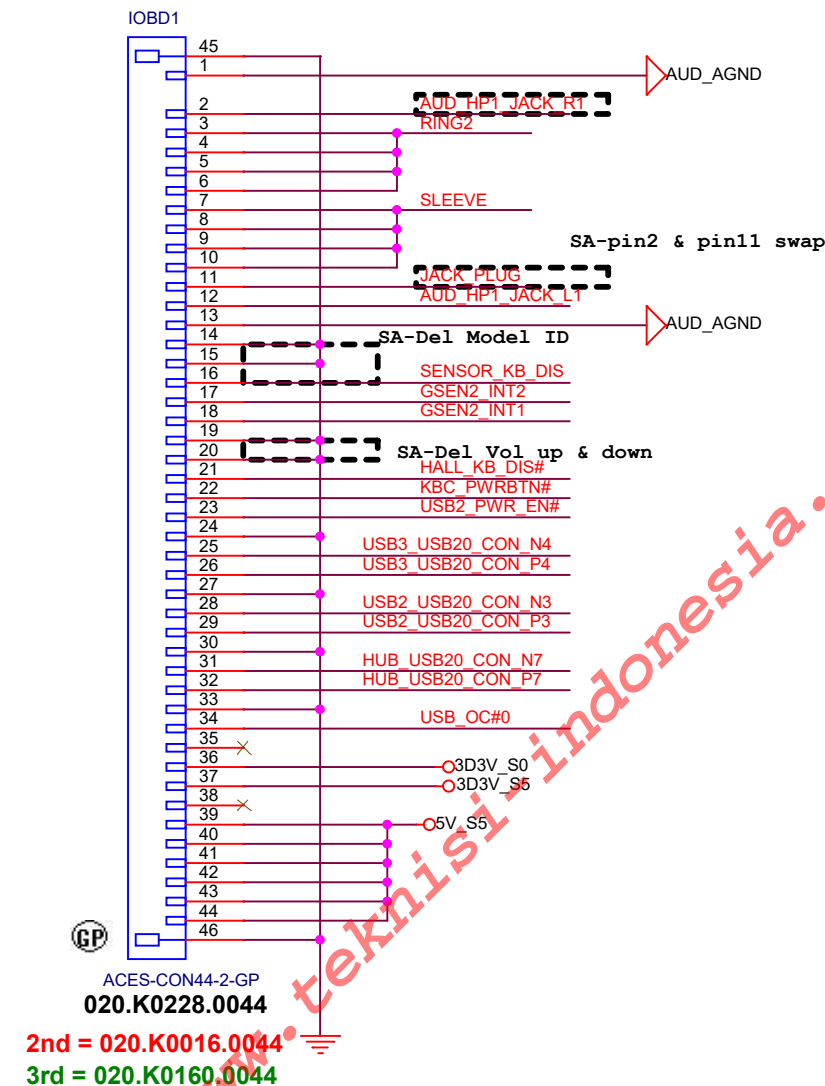
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LED / PWRBTN</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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# SSID = IO Connector

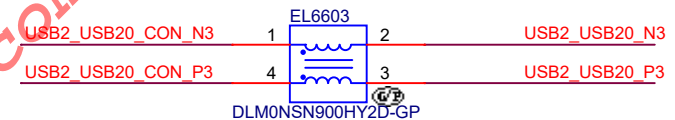
29	JACK_PLUG	<<<	---
29	RING2	<<<	---
29	SLEEVE	<<<	---
29	AUD_HP1_JACK_R1	>>>	---
29	AUD_HP1_JACK_L1	>>>	---
24	SENSOR_KB_DIS	<<<	---
69	GEN2_INT2	>>>	---
69	GEN2_INT1	>>>	---
24	HALL_KB_DIS#	<<<	---
24	KBC_PWRBTN#	<<<	---
24	USB2_PWR_EN#	>>>	---
17	USB_OC#0	<<<	---
16	HUB_USB20_P7	>>>	---
16	HUB_USB20_N7	>>>	---
16	USB2_USB20_P3	>>>	---
16	USB2_USB20_N3	>>>	---
16	USB3_USB20_N4	>>>	---
16	USB3_USB20_P4	>>>	---



068.09002.2001

2nd = 68.02002.061

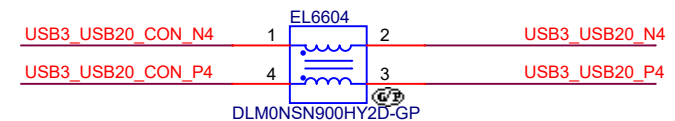
3rd = 068.00104.0001



068.09002.2001

2nd = 68.02002.061

3rd = 068.00104.0001

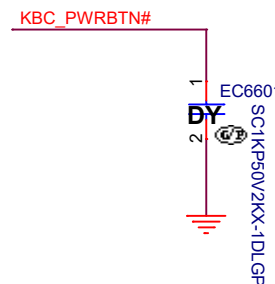


068.09002.2001

2nd = 68.02002.061

3rd = 068.00104.0001

USB2_USB20_CON_P3	1	AFTP6603
USB2_USB20_CON_N3	1	AFTP6602
USB3_USB20_CON_P4	1	AFTP6604
USB3_USB20_CON_N4	1	AFTP6605
3D3V_S0	1	AFTP6601
HUB_USB20_CON_P7	1	AFTP6607
HUB_USB20_CON_N7	1	AFTP6606



<Variant Name>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**IO Board CONN**

Size

Document Number

**JEAN GREY AMD**

Rev

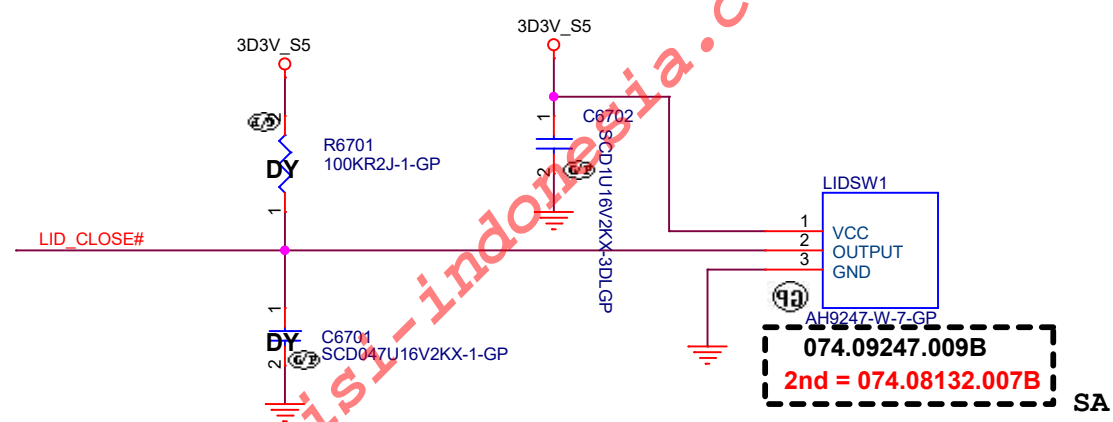
**A00**

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SSID = Hall Sensor

24 LID\_CLOSE# <<<—



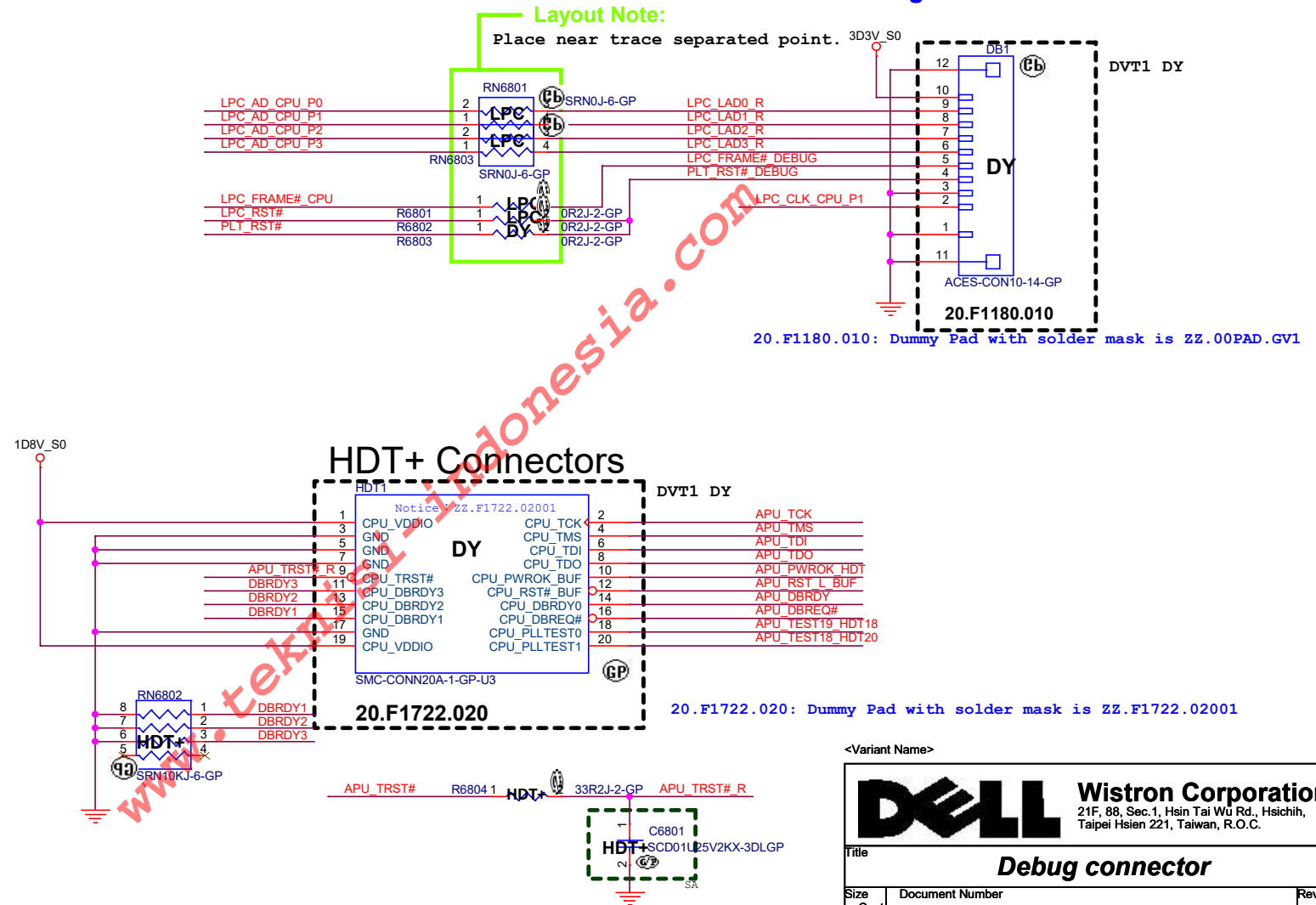
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Hall Sensor</b>			
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# SSID = DEBUG PORT

16,24 LPC\_AD\_CPU\_P0 <<>>  
16,24 LPC\_AD\_CPU\_P1 <<>>  
16,24 LPC\_AD\_CPU\_P2 <<>>  
16,24 LPC\_AD\_CPU\_P3 <<>>  
16,20,24 LPC\_FRAME#\_CPU <<>>  
  
16,24 LPC\_RST# >>>  
17,61,63 PLT\_RST# >>>  
16 LPC\_CLK\_CPU\_P1 >>>

8 APU\_TRST# <<>>  
8 APU\_TCK <<>>  
8 APU\_TMS <<>>  
8 APU\_TDI <<>>  
8 APU\_TDO <<>>  
8 APU\_PWROK\_HDT <<>>  
8 APU\_RST\_L\_BUF <<>>  
8 APU\_DBRDY <<>>  
8 APU\_DBREQ# <<>>  
8 APU\_TEST19\_HDT18 <<>>  
8 APU\_TEST18\_HDT20 <<>>



<Variant Name>



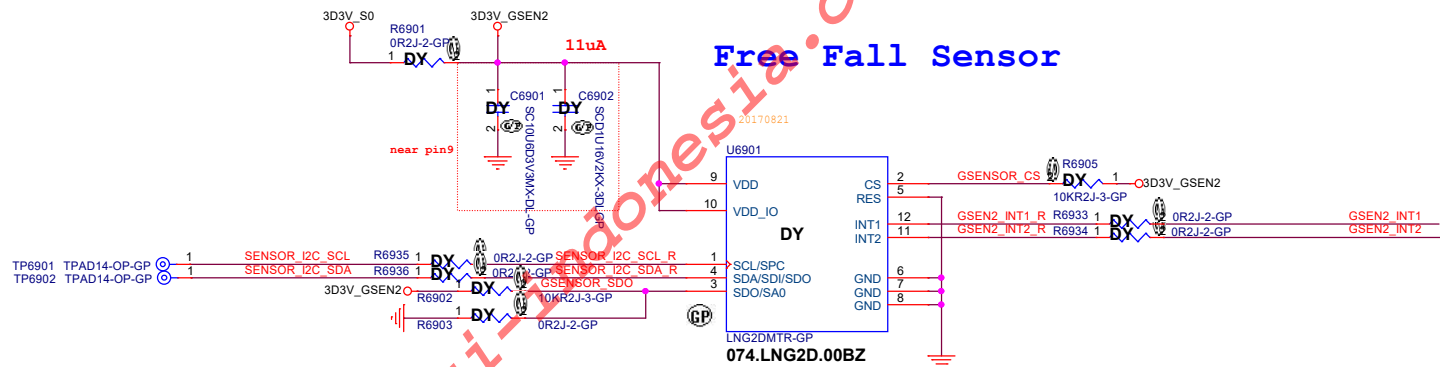
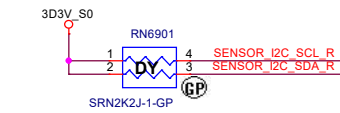
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			Debug connector
Size	Document Number	Rev	
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**SSID = Sensor**

24 GSEN2\_INT1 <<<\_\_\_\_\_

24 GSEN2\_INT2 <<<\_\_\_\_\_



## Free Fall Sensor



Title
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### ***FFS Sensor***

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Rev  
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Free Fall Sensor</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)Thunderbolt (1/5)</b>		
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<Variant Name>


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved) Thunderbolt (2/5)</b>		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)Thunderbolt (3/5)</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved) Thunderbolt (4/5)</b>		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)Thunderbolt (5/5)</b>		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)GPU (1/5) PEG</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)GPU (2/5) DIGITAL</b>		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)GPU (3/5) VRAM</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)GPU (4/5) GPIO</b>			
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<Variant Name>


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)GPU (5/5) PWR/GND</b>		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)VRAM1,2 (1/4)</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)VRAM3,4 (2/4)</b>			
Size A4	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)VRAM5,6 (3/4)</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)VRAM7,8 (4/4)</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)VGA_CORE</b>			
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)DISCRETE VGAPOWER</b>		
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<Variant Name>

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Title <b>(Reserved)</b>			
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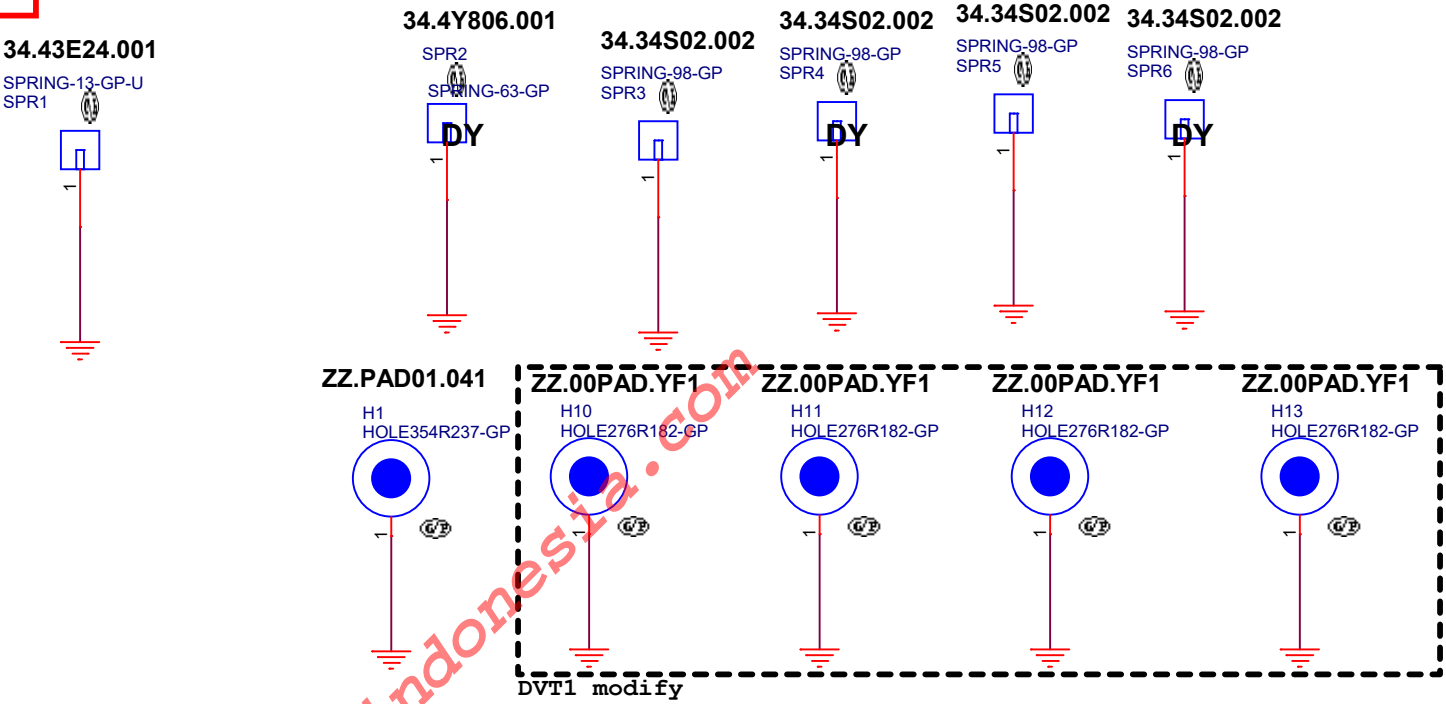
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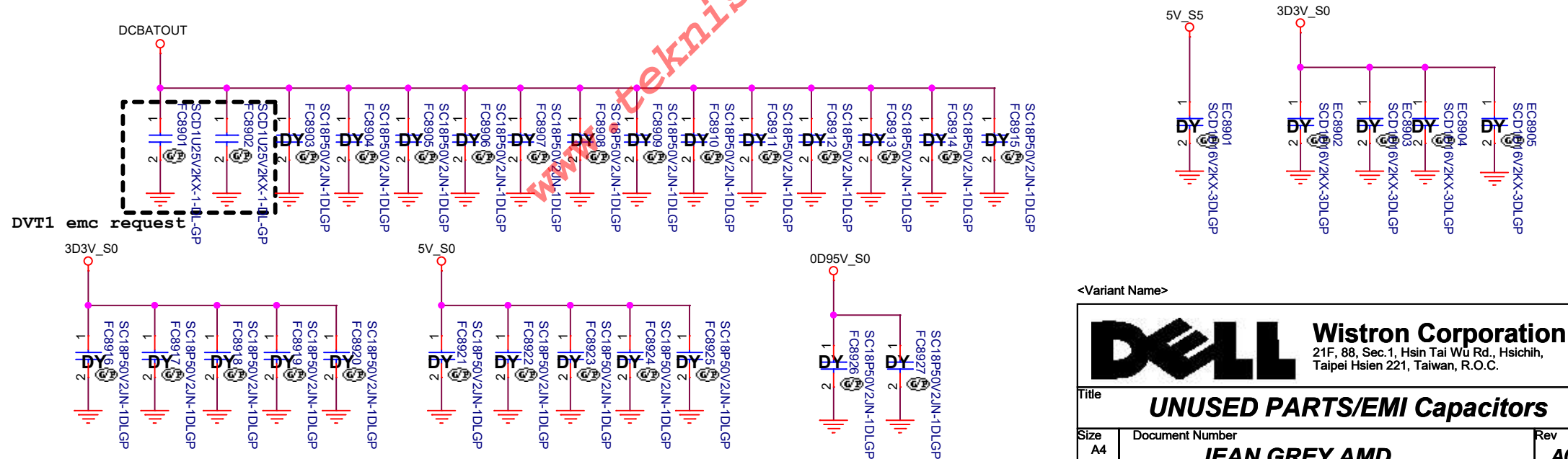
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Title <b>(Reserved)</b>			
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Main Func = UnusedParts



Main Func = EMI & RF Capacitors



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **UNUSED PARTS/EMI Capacitors**

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<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**(Reserved)NFC Connector**

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<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved) TPM**

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<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title **(Reserved)Finger Print**

Size A4	Document Number <b>JEAN GREY AMD</b>	Rev <b>A00</b>
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<Variant Name>

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Title <b>(Reserved)Express Card</b>			
Size A3	Document Number <b>JEAN GREY AMD</b>		Rev <b>A00</b>
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# Blanking

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<Variant Name>




**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
(Reserved)Smart Card Socket		
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<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)SW GFX eDP</b>		
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<Variant Name>


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)Bottom Docking</b>		
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<Variant Name>

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Title <b>(Reserved)</b>			
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<Variant Name>

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Title <b>(Reserved)</b>			
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<Variant Name>

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Title			
<b>CPU_XDP</b>			
Size	Document Number		Rev
A4	<b>JEAN GREY AMD</b>		<b>A00</b>
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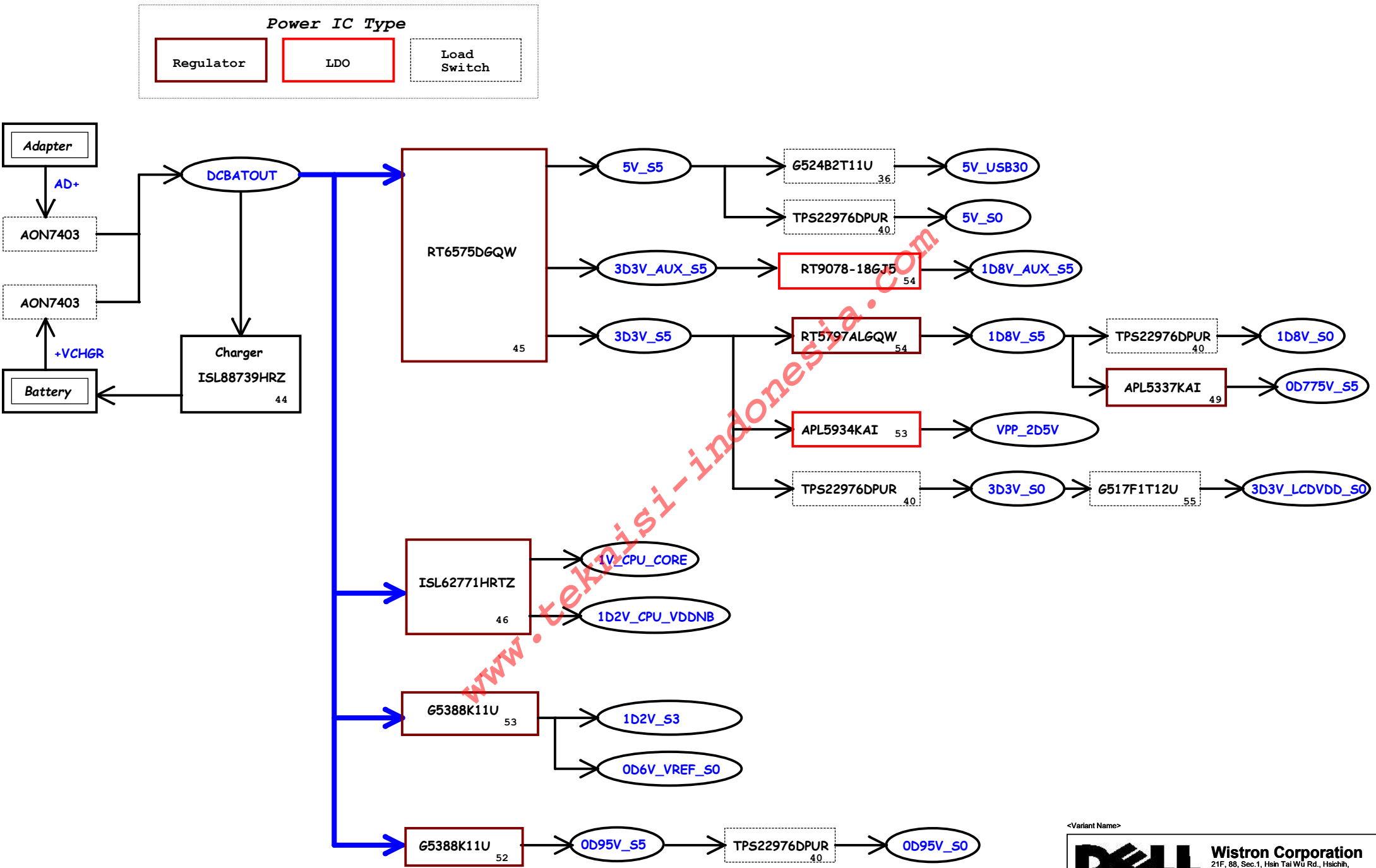
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001_Cover Page	037_(Reserved)	073_(Reserved)
002_Block Diagram	038_(Reserved)	074_(Reserved)
003_CPU (PCIE)	039_DISCHARGE	075_(Reserved)
004_(Reserved)	040_Power Plane Enable&Sequence	076_(Reserved) GPU (1/5) PEG
005_CPU (DDR)	041_(Reserved)	077_(Reserved) GPU (2/5) DIGITALOUT
006_(Reserved)	042_(Reserved)	078_(Reserved) GPU (3/5) VRAM I/F
007_CPU (VCC CORE)	043_DCIN JACK & BATT Conn	079_(Reserved) GPU (4/5) GPIO/STRAP
008_CPU (DISPLAY/SVI2/JTAG/TES)	044_CHARGER ISL88739	080_(Reserved) GPU (5/5) PWR/GND
009_CPU (VSS)	045_TPS51225RUKR 5V/3D3V	081_(Reserved) VRAM1,2 (1/2)
010_CPU (Power CAP1)	046_ISL62771 CPU CORE (1/2)	082_(Reserved) VRAM3,4 (2/2)
011_(Reserved)	047_ISL62771 CPU CORE (2/2)	083_(Reserved)
012_DDR4-SODIMM1	048_(Reserved)	084_(Reserved)
013_(Reserved) DDR4-SODIMM2	049_VDDCRGFX APL5337	085_(Reserved) GPU CORE ISL62771HRTZ
014_(Reserved)	050_(Reserved)	086_(Reserved) DISCRETE VGAPOWER
015_(Reserved)	051_(Reserved)	087_(Reserved)
016_CPU (CLK/SATA/USB/SPI/LPC)	052_APW8861 0D95V	088_(Reserved)
017_CPU (ACPI/SD/AZ/GPIO/RTC)	053_VDDQ&VTT&VPP APW8861	089_UNUSED PARTS/EMI Capacitors
018_(Reserved)	054_DC2DC 1D8V/1D5V	090_(Reserved)
019_(Reserved)	055_LCD/Inverter CONN	091_(Reserved)
020_CPU Strappings	056_(Reserved) VGA	092_(Reserved)
021_(Reserved)	057_HDMI	093_(Reserved)
022_(Reserved)	058_(Reserved)	094_(Reserved)
023_(Reserved)	059_(Reserved)	095_(Reserved)
024_KBC Nuvoton NPCE385	060_SATA IF HDD/ODD	096_(Reserved)
025_Flash (KBC+PCH) /RTC	061_NGFF WLAN CONN	097_(Reserved)
026_THERMAL NCT7718W/Fan	062_(Reserved)	098_(Reserved)
027_Audio Codec ALC3204	063_(Reserved)	099_(Reserved)
028_(Reserved)	064_LED Board&Power Button	100_Table of Content
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030_(Reserved)	066_IO Board Connector	102_Power Up Sequence Diagram
031_(Reserved) LAN RTL8111/RTL810	067_(Reserved)	103_Power Down Sequence Diagram
032_(Reserved) RJ45&Transformer	068_Debug connector	104_SMBUS BLOCK DIAGRAM
033_Card Reader	069_(Reserved)	105_THERMAL/AUDIO BLOCK DIAGRAM
034_(Reserved) USB2.0 CONN	070_(Reserved) Hall Sensor	106_CLK / USB Block Diagram
035_USB3.0 CONN	071_(Reserved)	
036_USB Power SW	072_(Reserved)	

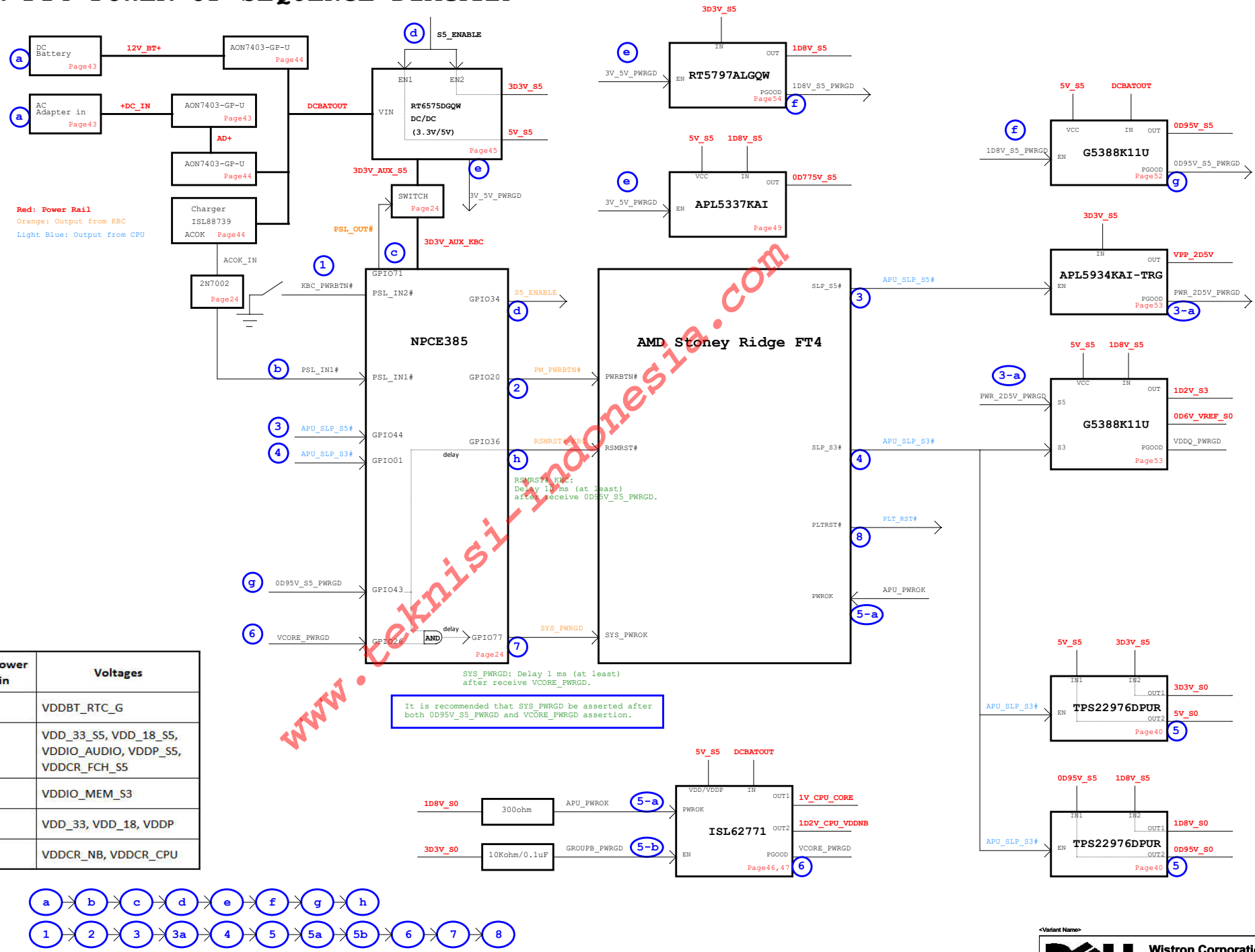
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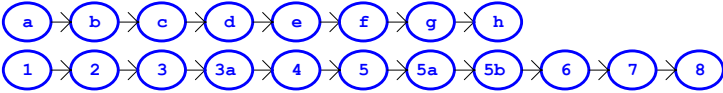
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Jean grey STR-FT4 POWER UP SEQUENCE DIAGRAM



Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_FCH_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_NB, VDDCR_CPU



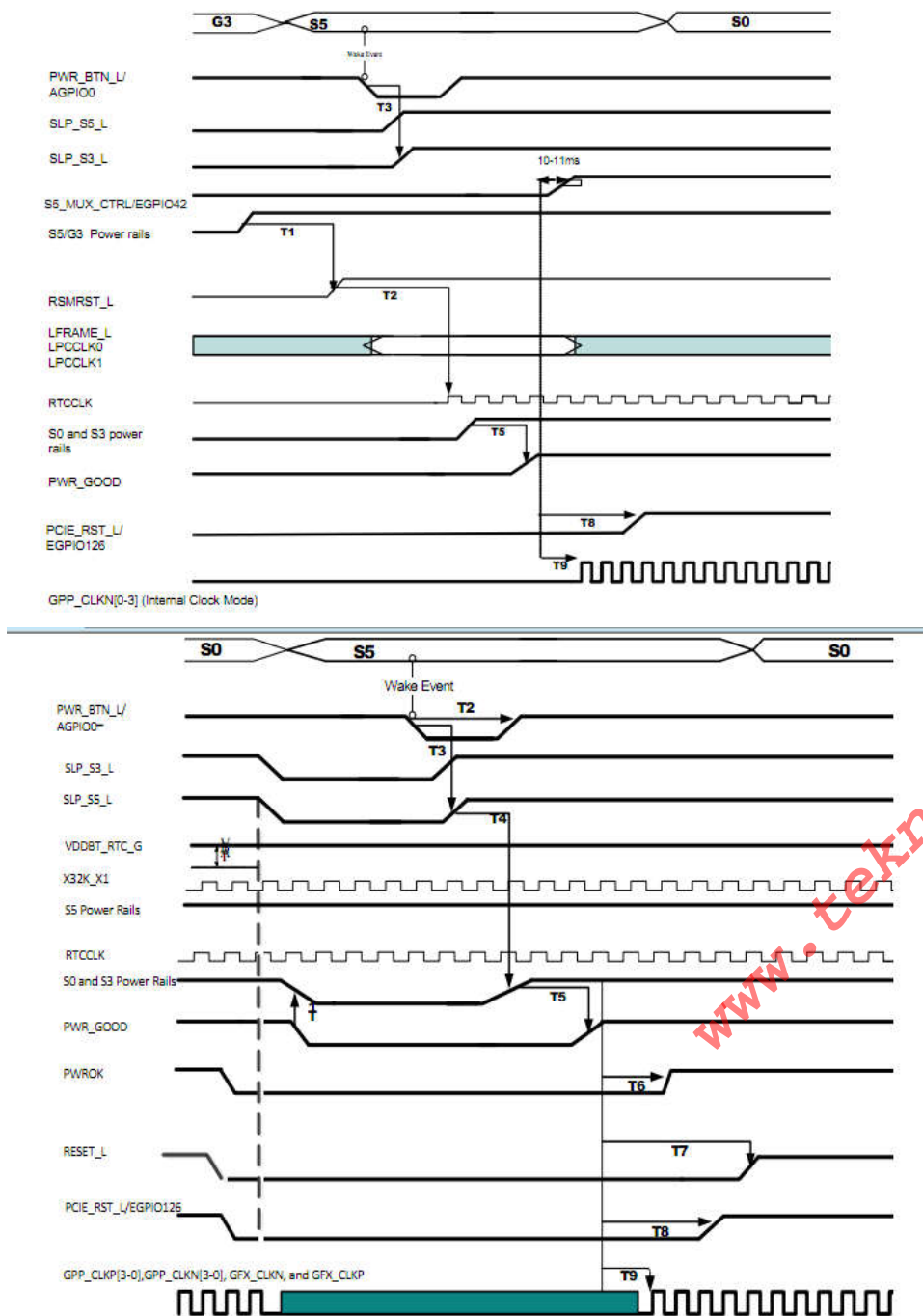


Figure 8. S0->S5->S0 Power Sequence Timing Diagram

Table 58. G3->S5->S0 Reset Sequencing Timing Parameters without coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L. *This could take up to 5 seconds if power has been removed from VDDBT_RTC_G.
T2	16.5ms		15.5ms	From RSMRST_L to RTCCLK. *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126 (rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

Table 59. G3->S5->S0 Reset Sequencing Timing Parameter with coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L.
T2	16.5ms			From RSMRST_L to RTCCLK. *This timing is only valid if a Schmitt trigger is used or RC time constant of 10ms is used.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising).
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126(rising).
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

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**Power Down Sequence**

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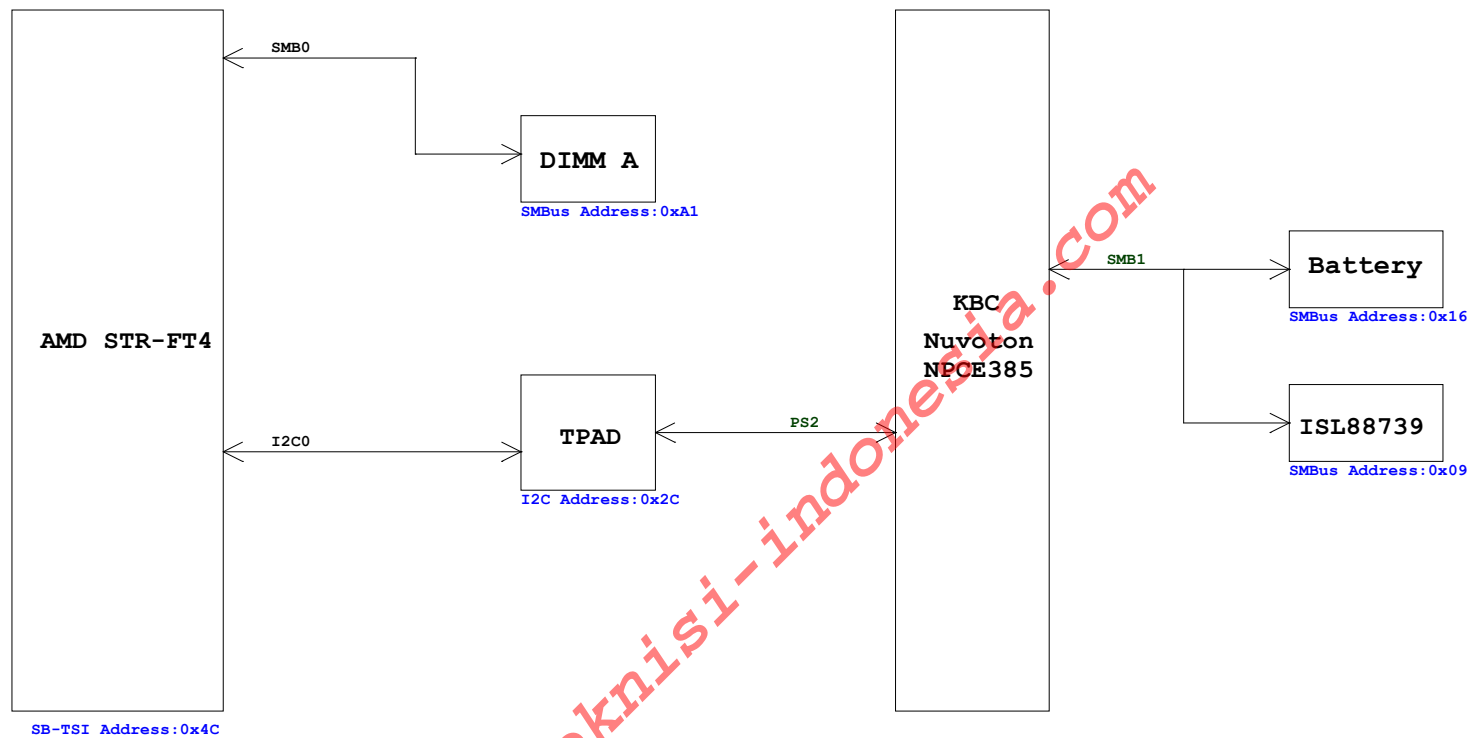
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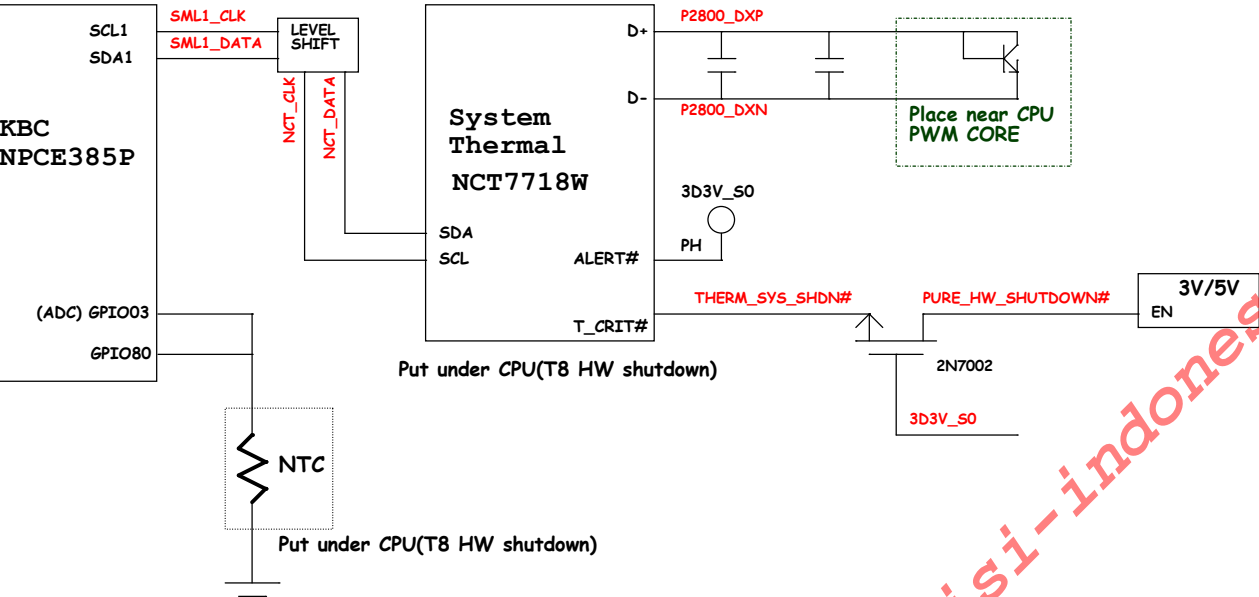


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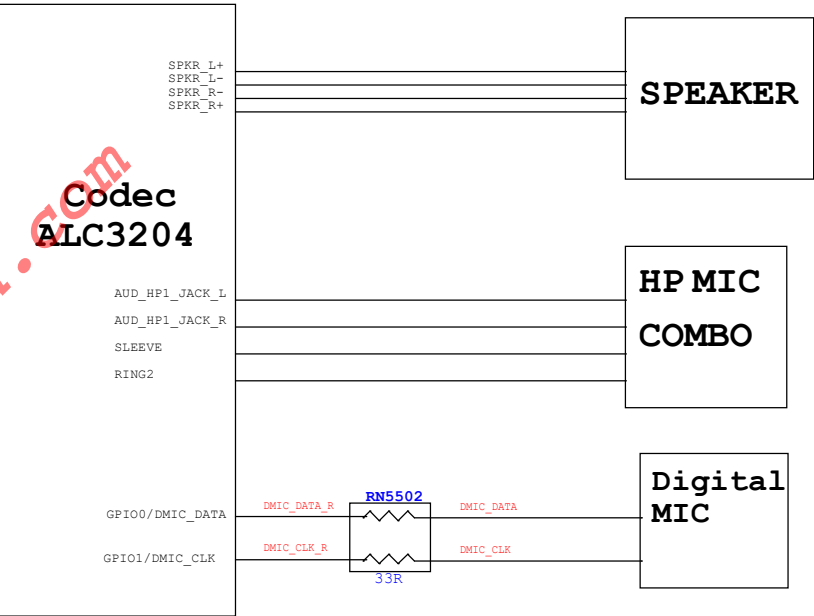
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# Thermal Block Diagram




# Audio Block Diagram



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<b>CLK / USB Block</b>		
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